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EDN

15 AUG 1986

SPECIAL ISSUE: Digital technology

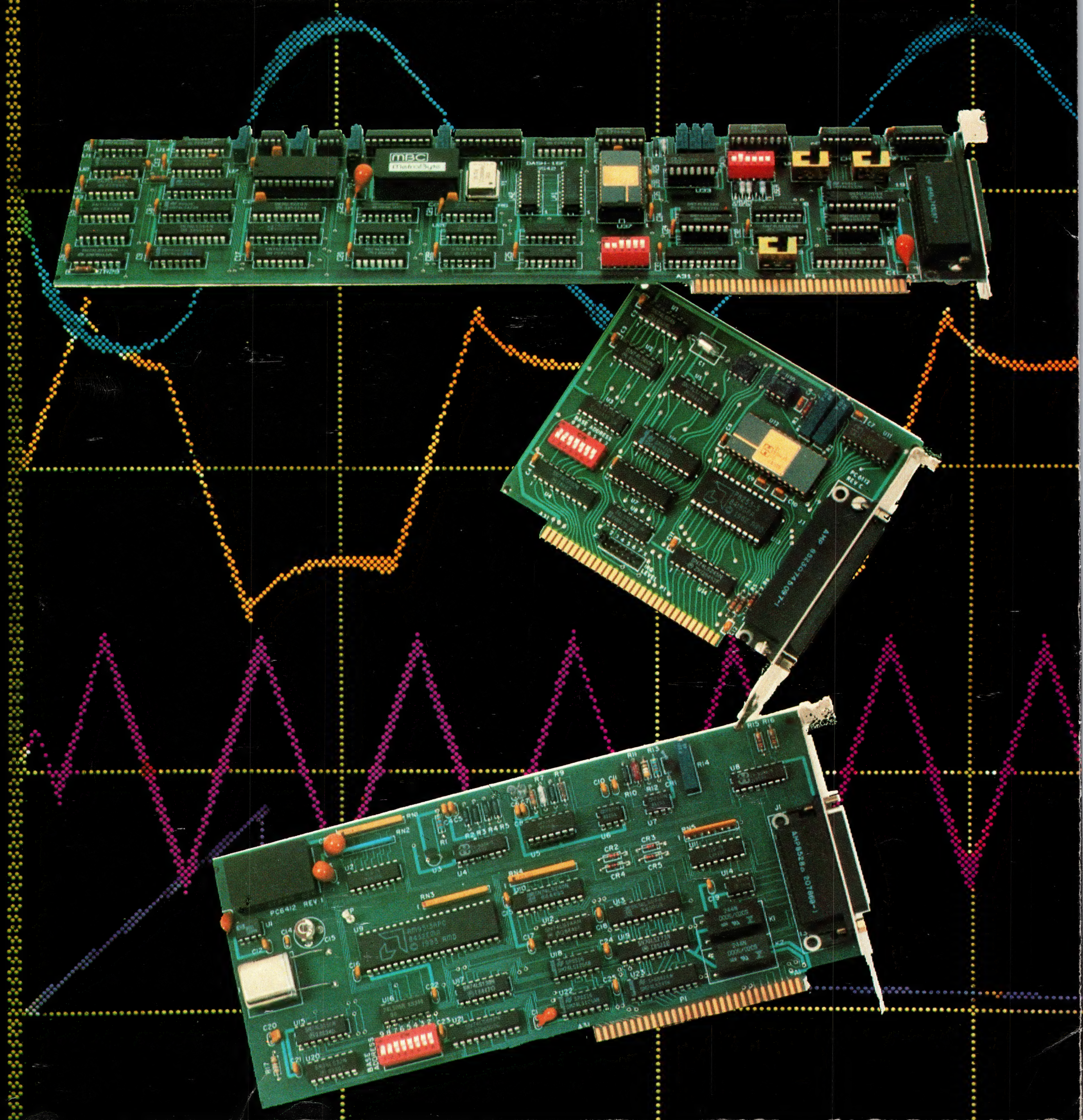
Floating-point-math chips support five companies' μPs

Clock/calendar chips bring time management to μCs

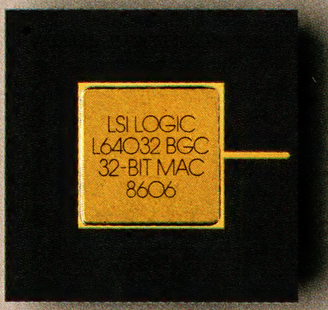
NCC '86 preview

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

I/O boards and software enable IBM to process and display analog sign



OR LEAVE WELL ENOUGH ALONE.



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Now it's hours.

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MAC for short.

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And none of this would be possible without our MACGEN Megacell Compiler. The newest addition to our proven, proprietary LDS software. Which lets you design faster VLSI circuits in one-tenth the time of previous methods.

The choice is yours. Pick up the phone and have your L64032 MACs in minutes. From us or our distributors.

Or stop by our design centers. And let's start on your custom or structured-array MAC.

If you can spare an hour.

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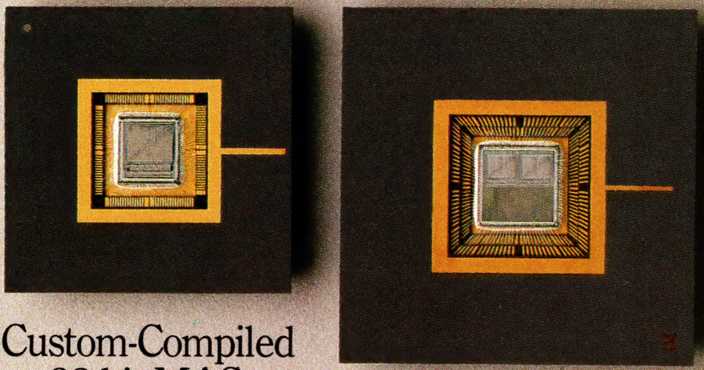
For more detailed information on the L64032 MACs or MACGEN, call 408-433-7454. *Distributors:* Hall-Mark; Hamilton/Avnet; Schweber; Wyle. *LSI Logic Sales Offices and Design Centers:* Milpitas, CA 408-433-8000, San Jose, CA 408-248-5100, Irvine, CA 714-261-0124, Sherman Oaks, CA 818-906-0333, Denver, CO 303-756-8800, Westport, CT 203-222-9336, Altamonte Springs, FL 305-339-2242, Boca Raton, FL 305-395-6200, Norcross, GA 404-448-4898, Chicago, IL 312-773-0111, Waltham, MA 617-890-0161, Ann Arbor, MI 313-769-0175, Minneapolis, MN 612-835-6161, Poughkeepsie, NY 914-454-6593, Raleigh, NC 919-872-8400, Trevose, PA 215-638-3010, Austin, TX 512-343-4513, Dallas, TX 214-788-2966, Bellevue, WA 206-455-5055, Calgary, Alta 403-262-9292, Kanata, Ont 613-592-1263, Paris, France 33-1-46-20-65-92, Israel 972-52-446594, Tokyo, Japan 81-3-589-2711, Osaka, Japan 81-6-947-5281, Sweden, 46-8-520720, United Kingdom, 44-344-426544, Munich, West Germany 49-89-926903-0, Düsseldorf, West Germany 0211-5961066, Stuttgart, West Germany 011-49-711-2262151. MACGEN, LDS, Megacell Compiler and Structured Array are trademarks of LSI Logic Corporation. ©1986 LSI Logic Corporation.

CIRCLE NO 207

NOW YOU CAN CUSTOM BUILD A 32-BIT MAC IN ONE HOUR.



Custom-Compiled 32-bit MAC.

Structured Array with two MACs.

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What instrument is no bigger than a lunchbox, takes measurements like four high-performance multimeters, gathers data like a logger, and stores tens of thousands of readings?

Only one instrument is like that—Wavetek's new Model 52 Data Multimeter.

It measures DC voltage and current, AC voltage (to 1 MHz) and current, resistance, volt-amperes, dB, frequency, period, time interval and pulse width. And it accepts industry-standard thermocouples—J, K, E and T.

The data is shown in numeric and/or bar graph form on the large, high-resolution LCD. The display also helps with setup by providing complete menus for every function.

Four parallel, isolated A-D channels let the Model 52 do the work of four ordinary DMMs. Built-in computing functions calculate deltas, percentages, minimum/maximum readings and averages and detect alarm thresholds. You can even program your own math functions.

Model 52 is also a data logger. Add optional multiplexers and you can gather up to 252 channels of analog data and store the readings in nearly a megabyte of RAM. Digital I/O options add up to 32 bits of digital input and output as well as D/A capability for external control applications.

Internal batteries protect your data and provide total portability. Leave it on a mountaintop and gather data for months, or put it in a plane and take readings on the fly.

The Model 52 is easy to live with. You can transfer data to any computer's database at your convenience using the standard RS-232 or optional IEEE-488 interface. Unique Flex-Cal closed-box calibration saves your valuable time.

Surface-mounted devices and a custom gate array make it possible to offer all these features in such a compact package—and a very low price. Also available is the remote-only Model 51 for an even lower price.

For more information, call us at (619) 279-2200, or write Wavetek San Diego, Inc., 9045 Balboa Ave., P.O. Box 85265, San Diego, CA 92138. TWX 910-335-2007.

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Circle 5 for Literature

Circle 44 for Demonstration

STANDARDS UPDATE

FCC EMISSIONS — COMPUTERS, PERIPHERALS AND ELECTRONIC EQUIPMENT

Sanctions are expected in the wake of spot checks on 29 computers from 22 manufacturers showing that **half** failed to comply with FCC rules. Part 15 of these rules requires that nearly all electronic equipment be tested for compliance with the regulations. Penalties can range from fines of $2,000 per day to imprisonment of up to one year and seizure of non-compliant goods. Many of the machines were bought from distributors by FCC representatives. The tests were conducted by the FCC's Sampling and Measurement Branch, a new watchdog section of the FCC.

Continuing tests for compliance are required by the FCC rules. Many of the 29 devices tested by the Sampling and Measurement Branch had previously been certified by the Commission. FCC rules in Part 2, and under its April 7, 1982, Public Notice, require manufacturers not only to have prototypes tested, but also to demonstrate that devices continue to comply. Changes must be evaluated by qualified engineers to determine if retesting is necessary. Documentation on all changes must be in order.

FCC compliance at a guaranteed rate by a guaranteed date is promised by Dash, Straus & Goodhue, Inc. (617-263-2662), the Northeast's largest research and development firm dedicated to EMI, ESD and Telecom compliance. Under that program, a customer can call DS&G and receive, over the phone, a commitment to have a device tested, modified (if necessary), retested and verified within a guaranteed time for a guaranteed rate. **DS&G's in-house legal staff** prepares, in complete confidence, all necessary applications to the FCC. That legal staff is prepared to assist clients, should the FCC call.

TELECOM REGULATIONS

Japan's marketplace is now open. Intensive efforts on the part of the Reagan administration have succeeded in opening the Japanese telecommunications market "in principle." But tests for compatibility with Japan's telecommunication networks require considerable expertise.

DS&G now tests for Japanese Telecom. Dash, Straus & Goodhue has announced that it is now testing equipment for compliance with Japanese telecommunications regulations. DS&G's legal counsel based in Japan hand-carry all applications through Japanese authorities. This complete Japanese Telecom program, together with DS&G's U.S. and Canadian efforts, gives manufacturers the ability to market in three countries through a single laboratory.

FCC rules expand to cover digital. Devices using T1 (1.544 M bit) and subrate lines, as well as certain types of test equipment, now require FCC registration. New requirements are part of a continuing process of expanding FCC rules, Part 68, to cover nearly all devices which can hook to the network.

SAFETY

An insurance crisis looms for product liability. Premiums have skyrocketed as insurers attempt to cover costs related to steeply rising legal claims. Manufacturers of electronic equipment, many of whom have to forego liability insurance, must now look even closer at the safety of the products they sell.

UL® listing may be the best protection. Listing, while not a complete defense, makes hostile litigation far less likely. Also, many insurance policies are void without it.

CSA®, UL® and West German approval at one location is now possible through work at Dash, Straus & Goodhue. Combining engineering, in-house test capability and legal skill, DS&G can package submissions simultaneously for all three safety approvals. Final tests carried out by these organizations are co-ordinated through DS&G.

COMPLIANCE DESIGN INC. ANNOUNCES A NEW PART 68 WORKSTATION™

The Workstation is designed for complete evaluations of telephones, modems, key systems and PBXs for compliance with FCC, DOC and EIA standards. The Workstation tests include: (1) hazardous voltages and currents, (2) signal power limitations, (3) balance, (4) impedance limitations, (5) billing protection, and (6) surge. By putting all this technology together in a single unit, Compliance Design has made testing to the specifications simpler and easier than with jury-rigged collections of equipment now used in many locations. For detailed information, circle the Compliance Design Reader Service Number below.

COMPLIANCE ENGINEERING 1987 NOW AVAILABLE — FREE OF CHARGE

Rapidly becoming the industry's standard handbook of EMI, ESD, Telecom and Safety compliance, ***Compliance Engineering 1987*** will cover both specifications and methods of engineering for compliance. The handbook is available free of charge by circling the Reader Service Number below.

All inquiries handled in complete confidence.

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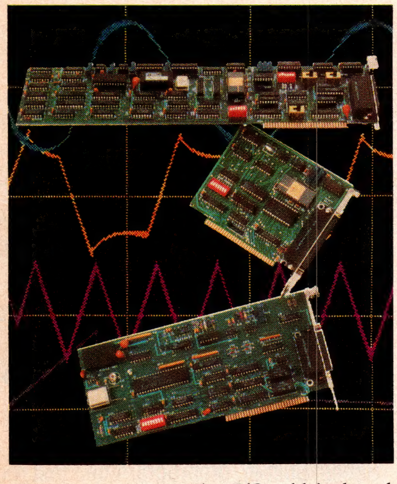
Volume 31, Number 12

EDN

June 12, 1986

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Analog-I/O add-in boards for the IBM PC, PC/XT, and PC/AT are offering high throughput rates as well as functions like DMA data-transfer capability. Moreover, software packages—from the board manufacturers as well as from third-party vendors—make the boards easy to control. See pg 116. (Photo courtesy Metrabyte)*

DIGITAL TECHNOLOGY SPECIAL ISSUE

DESIGN FEATURES

Continued on page 7

EDN (ISSN 0012-7515) is published 45 times a year, biweekly with one additional issue in January, February, March, August, and December, two additional issues in April, June, July, September, and November, and three additional issues in May and October by Cahners Publishing, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158. William M Platt, President; Terrence M. McDermott, Executive Vice President; Jerry D. Neth, Vice President of Publishing Operations; J.J. Walsh, Financial Vice President/Magazine Division; Thomas J. Dellamaria, Vice President Production & Manufacturing; Terrence McDermott, Group Vice President. Copyright 1986 by Reed Publishing USA, a division of Reed Holdings, Inc; Saul Goldweitz, Chairman; Ronald G Segel, President and Chief Executive Officer. Circulation records maintained at Cahners Publishing Co, 270 St Paul St, Denver, CO 80206. Second class postage paid at Denver, CO 80202 and additional mailing offices. Postmaster: Send address changes to EDN, 270 St Paul St, Denver, CO 80206.

If you can't fix your board with the enhanced 9000 Series, it's beyond repair.

Introducing a new dimension of test capabilities for the Fluke 9000 Series Micro-System Troubleshooter line.

Finally there's a way to conquer some of the most difficult board testing problems imaginable. Take control of the situation with Fluke's 9000 Series and new **Asynchronous Signature Probe option.** You'll be able to pinpoint virtually every digital hardware fault on the entire board. Even those frustrating faults in circuits that operate independently of the microprocessor bus cycle.

Begin testing boards with the 9000 Series' built-in, preprogrammed test routines. In a single keystroke, you can automatically check the entire microprocessor kernel—Bus, ROM, RAM and I/O.

For testing beyond the bus, Fluke's new probe option eliminates the need for a logic analyzer or scope to test asynchronous circuits. One complete package, easily installed into either new *or* existing 9000 Series units, offers signature analysis, waveform capture and event counting. These three vital troubleshooting functions give *any* 9000 Series the power to diagnose:

- DMA Controllers
- Disk Controllers
- Video Controllers
- Video-Generation Circuits
- Communication Circuits
- Peripheral Controllers
- Dynamic RAM timing relationships

Not only does the 9000 Series test more of the board, it also supports more 8-bit and 16-bit processors than any other tester on the market.

Call Fluke toll-free **1-800-426-0361** or contact your local representative, and put your most challenging board to the 9000 Series test. If it can't be fixed with the enhanced 9000, it's probably beyond repair.

FLUKE®

IN THE U.S. AND NON-EUROPEAN COUNTRIES: John Fluke Mfg. Co., Inc., P.O. Box C9090, M/S 250C, Everett, WA 98206, Sales: (206) 356-5400, Other: (206) 347-6100.
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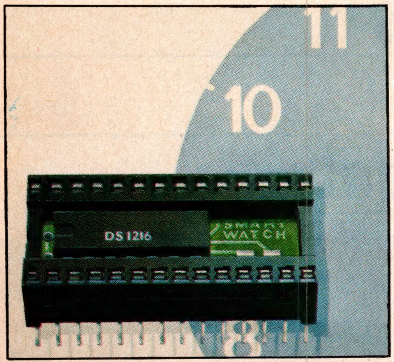
EDN

June 12, 1986



***Up-to-date clock/calendar ICs** simplify system design (pg 73).*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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SYSTEMS DVMs

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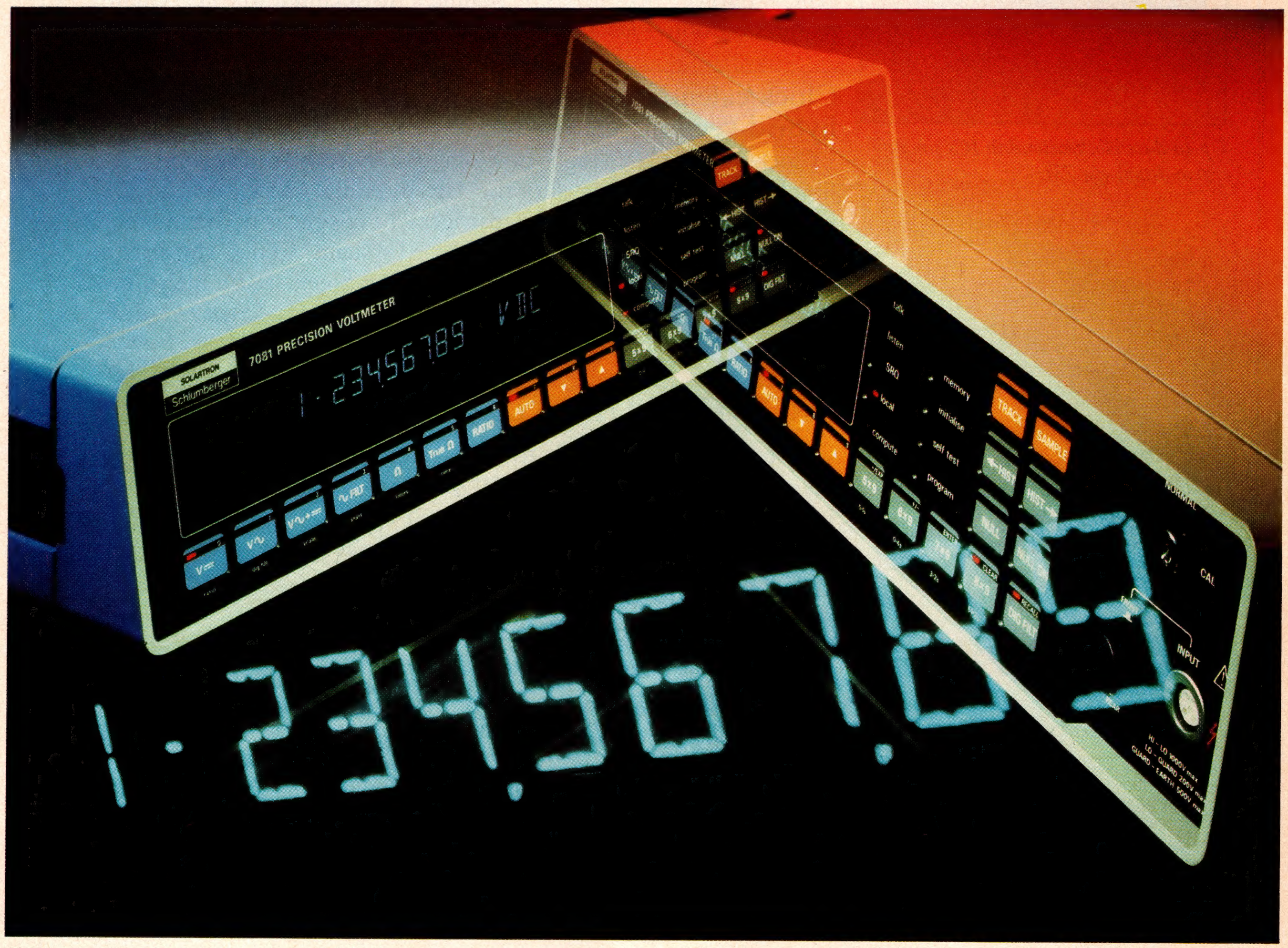

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Function	Range	Accuracy 7081 (8½)	Accuracy 7071 (7½)
Volts dc	10 nV to 1000V	1.2 ppm/24 hr. 11ppm/1yr. 33 ppm/9yr	3ppm/24hr. 20ppm/1yr 66ppm/9 yr.
Volts, true rms ac	1μV to 750V	150 ppm	150 ppm
Ohms	10Ω to 1000MΩ	1.5ppm	1.5ppm
Transfer Accuracy		0.3ppm	1ppm
Linearity		0.3ppm	0.5ppm

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CIRCLE NO 10

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EDITORIAL 51

Let me tell you about the Money Stream Theory: A money stream runs through every company; money comes in (revenue), and money goes out (expenditures). The closer you are to the incoming flow, the higher your salary, position, and prestige are likely to be. The closer you are to the outgoing flow, the bleaker your prospects. Sad to say, this theory is true.

NEW PRODUCTS

PROFESSIONAL ISSUES 290

Engineering students name companies for which they'd most like to work.—*Deborah Asbrand, Staff Editor*

LOOKING AHEAD 300

μPs to spur $1.13B market for data converters . . . VLSI IC design centers to gain share of ASIC design.

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SIEMENS

GRAND PRIX for "Micro-boards"

Favourite: Central Computer Unit SMP-E 19-A8

Good news from the Modular Microcomputer Board System SMP:
The Central Computer Unit SMP-E 19-A8 is the favourite in the microcomputer grand prix for compact single euroformat boards.
It has the following SMP characteristics, time tested in numerous industrial applications.

- SMP bus
- Standard Euroformat (100 x 160 mm)
- Indirect Connections
- Multilayer Board

These characteristics are combined with the 16 bit world through:

- 8 MHz SAB 80188 Central Processor
- 128 Kbyte dynamic RAM
- up to 64 Kbyte EPROM
- Serial and Parallel Input/Output
- Interupt and DMA Control
- Timer/Counters

Whether in mechanical engineering laboratory and testsystems or in general control and measurement applications: The Central Computer Unit SMP-E 19-A8 makes problem solving easier and in addition, supports 110 other functions in the SMP product spectrum.

The Microcomputer Board Systems from Siemens AMS – SMP – PMS

You save:
Time: – Through use of existing hardware
Money: – Through use of previously acquired know-how
Work: – Through application of existing documentation and production plans.

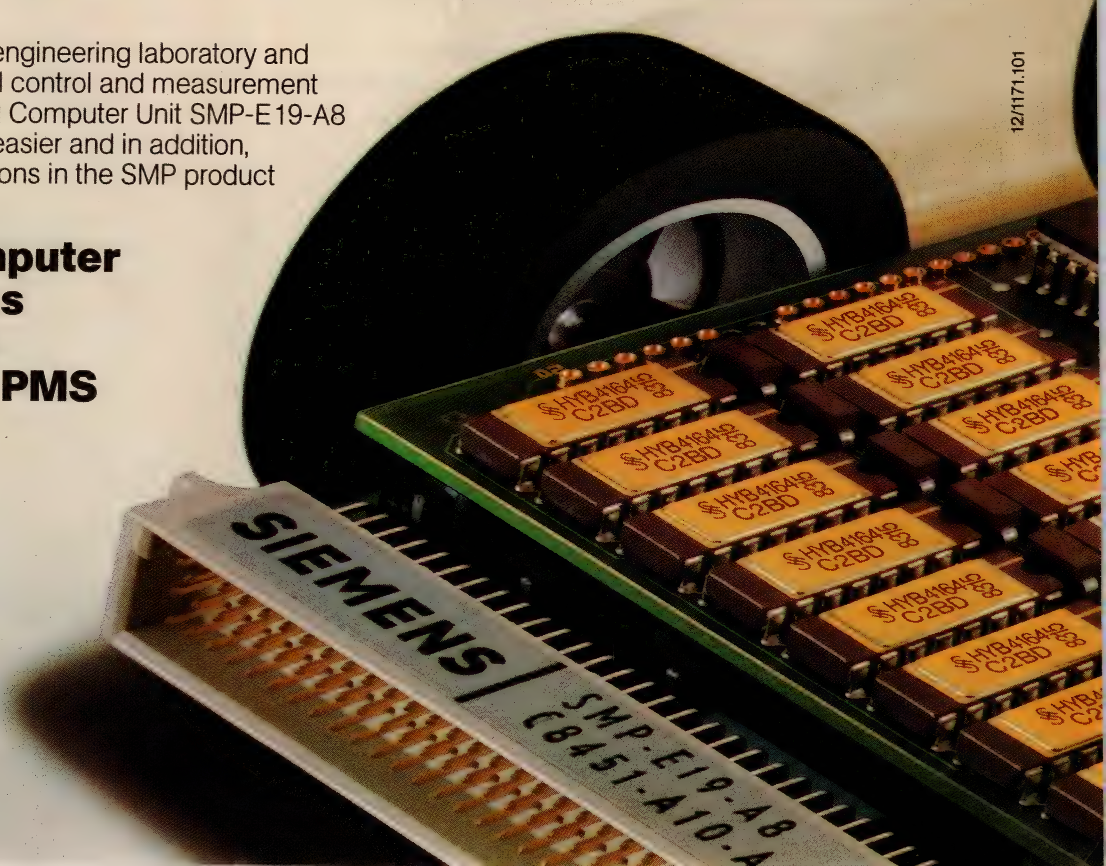
These savings mean you gain your share of the market faster, because your products can be released earlier.

Stop press: A central computer unit SMP-E 18-A8 with static CMOS RAM and differing I/O features is in preparation. This board is well suited for areas where dynamic RAMs are not suitable.

Would you like to know more?

Ask your Siemens Components Team. Or send for complete information from Siemens AG, Infoservice 12/1171, Postfach 23 48, D-8510 Fürth.

12/1171.101



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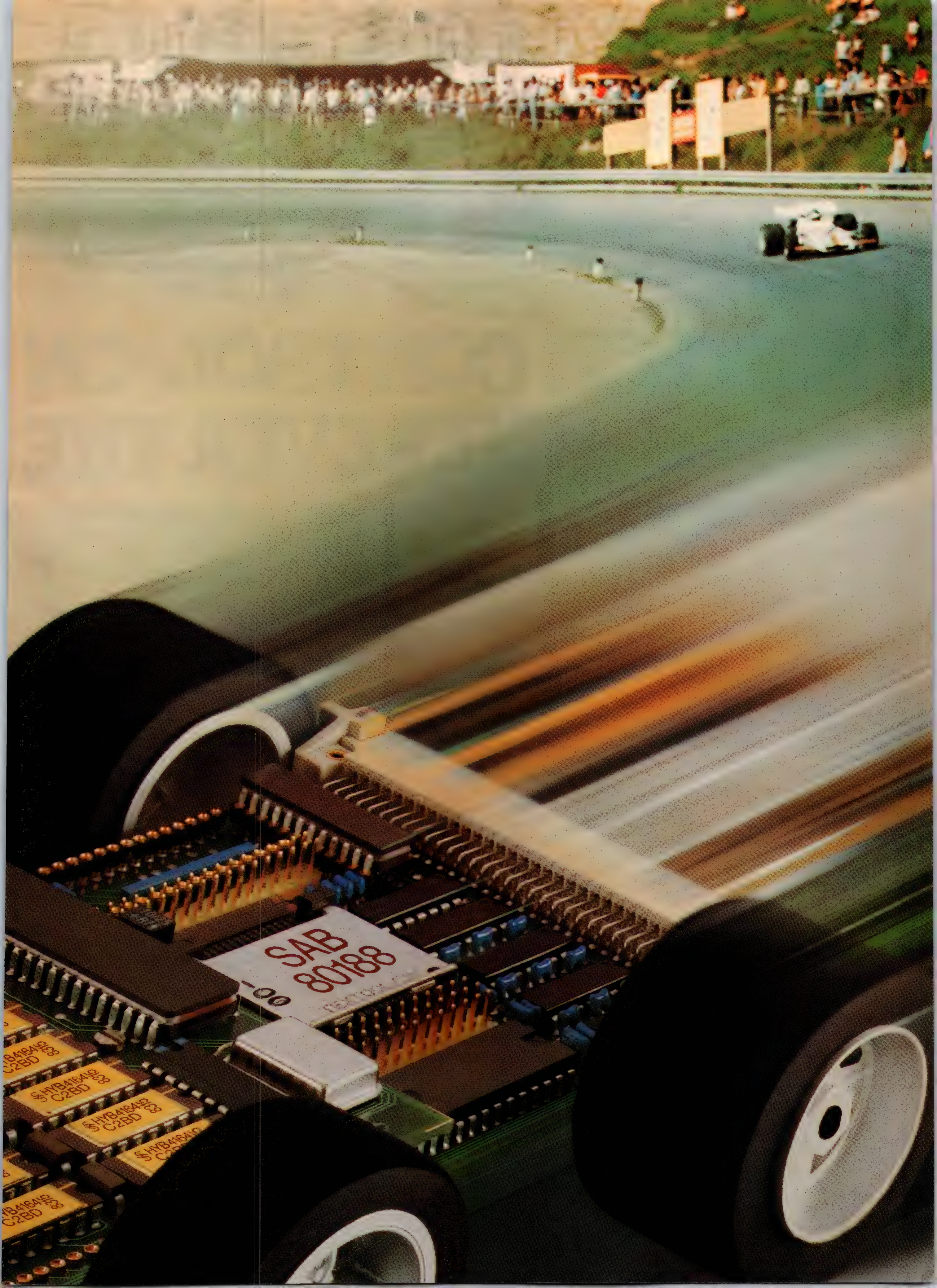
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Designing control systems? When it comes to automation, robotics, and microprocessor-based instruments and equipment, better tools make better systems. Faster. What we offer are better tools, proven technology, and familiar software environments.

Better hardware. Ziatech's advanced STD Bus boards allow you to configure microcomputer control systems your way. 8088 and 80188-based CPU's and Single Board Computers running at speeds up to 8MHz. Memories to 1 Mbyte. Disk Controller, General Purpose I/O and IEEE 488 Controller Boards. Plus Multimodules and Accessories. Each with a 24-month warranty. It's the hardware you need to develop complete control systems. Modularly.

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STD polyFORTH,™ STD VRTX™ and STD DOS,™ our implementation of IBM PC-DOS. It means you can develop software in a familiar IBM PC environment. And unlike some other supposed STD Bus DOS offerings, Ziatech software won't turn your PC-AT into a dumb terminal. What's more, you'll have access to a vast library of development tools written for MS and PC-DOS. Tools that can have your system up and running. Fast.

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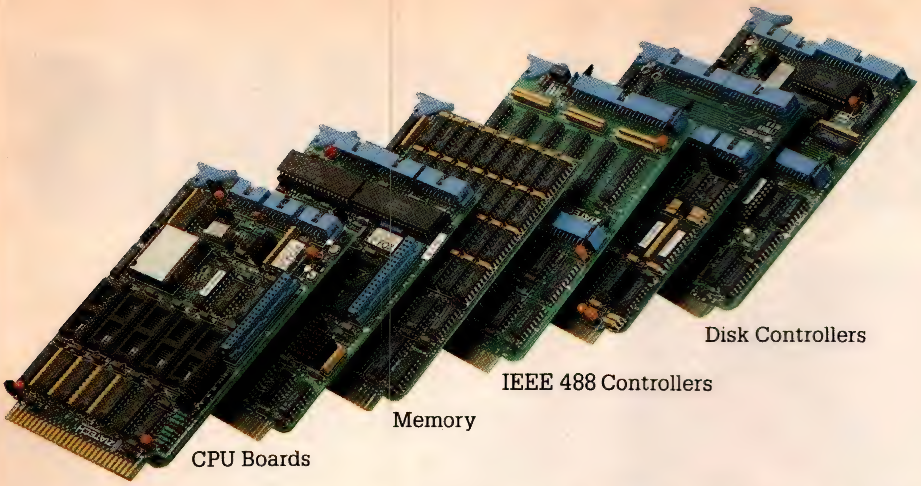

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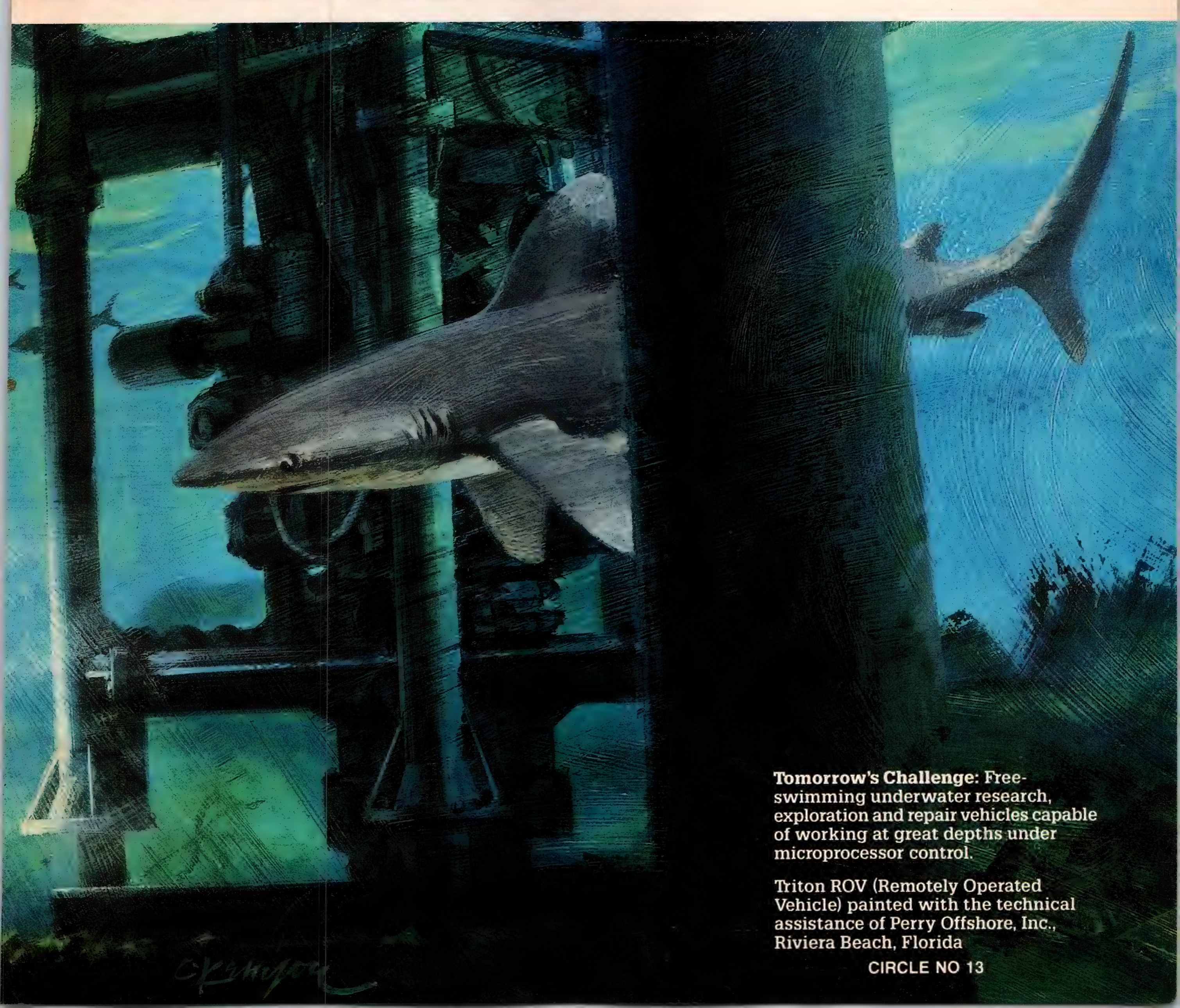
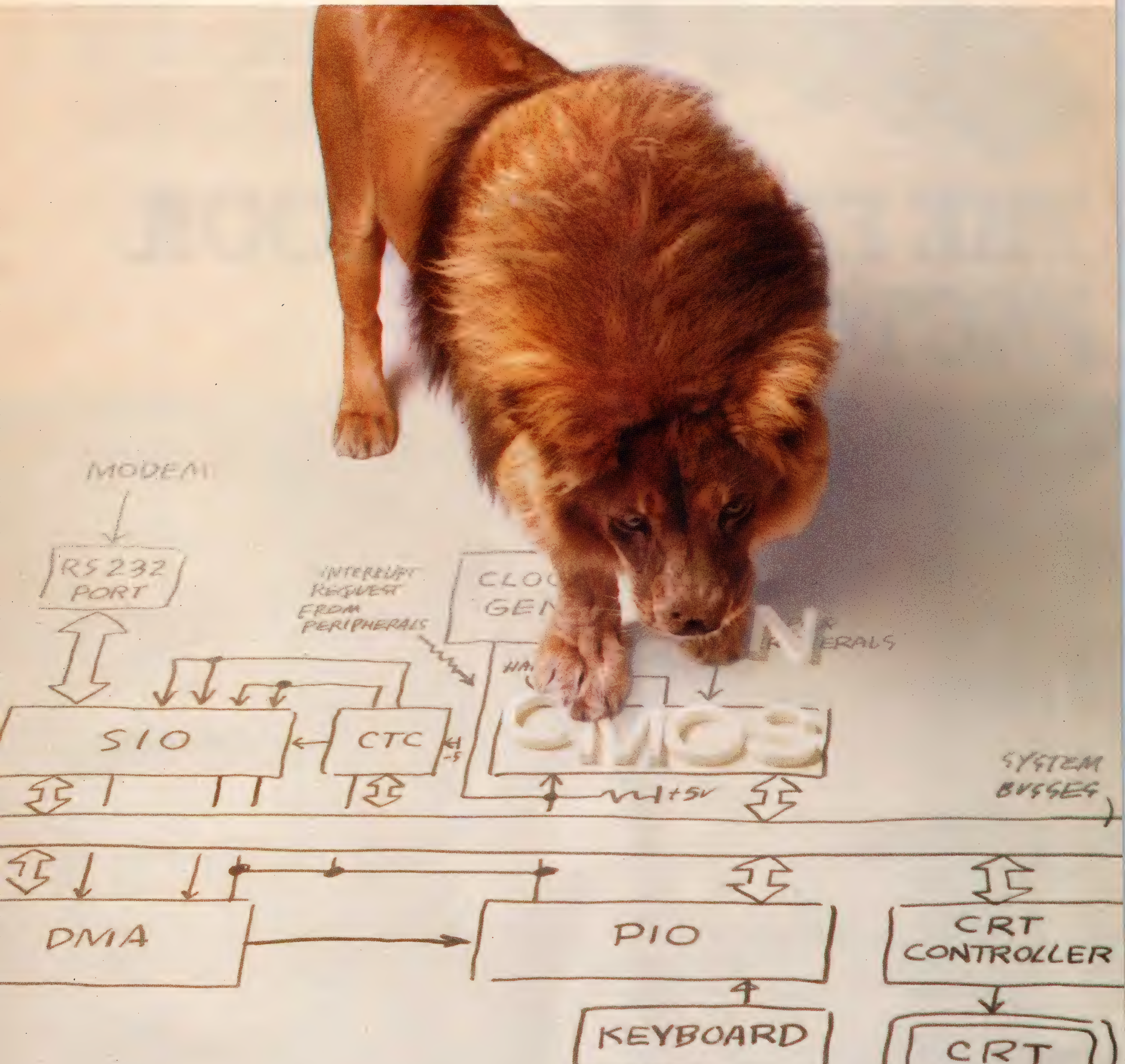


Tomorrow's Challenge: Free-swimming underwater research, exploration and repair vehicles capable of working at great depths under microprocessor control.

Triton ROV (Remotely Operated Vehicle) painted with the technical assistance of Perry Offshore, Inc., Riviera Beach, Florida

CIRCLE NO 13

TOSHIBA CMOS



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Device	Description	Technology	Operating Current at 4MHz	Power-Down Current
TMPZ84C00	4MHz Z80A CPU	CMOS	15mA	$<10\mu A$
TMPZ84C30	CTC: Counter/Timer Circuit	CMOS	3mA	$<10\mu A$
TMPZ84C20	PIO: Parallel Input/Output Controller	CMOS	2mA	$<10\mu A$
T6497	Clock Generator/Controller	CMOS	2mA	$<10\mu A$
TMPZ84C40	SIO: Serial Input/Output Controller	CMOS	25mA	$<10\mu A$
TMPZ84C10	DMA: Direct Memory Access Controller	CMOS	25mA	$<10\mu A$

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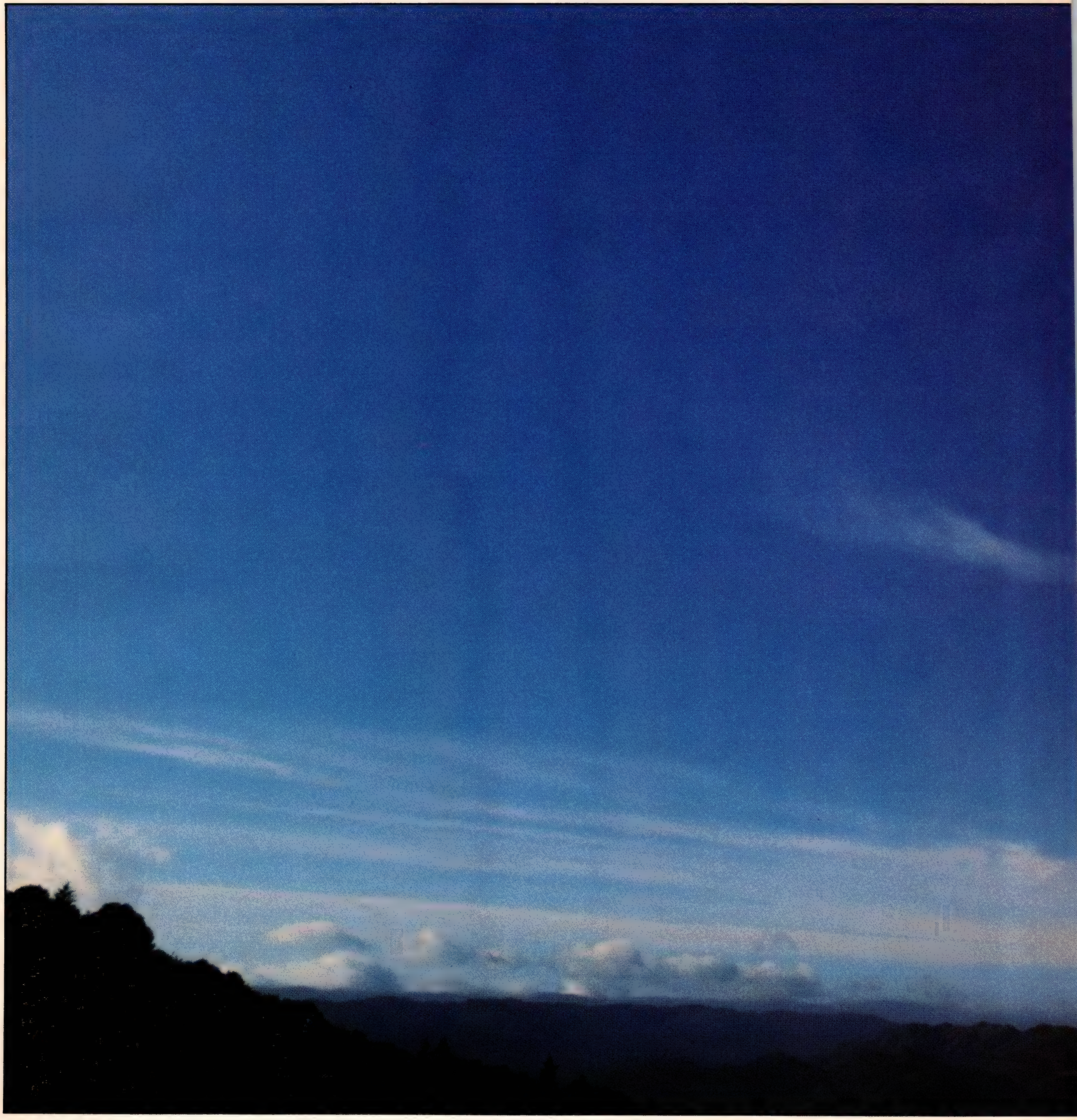

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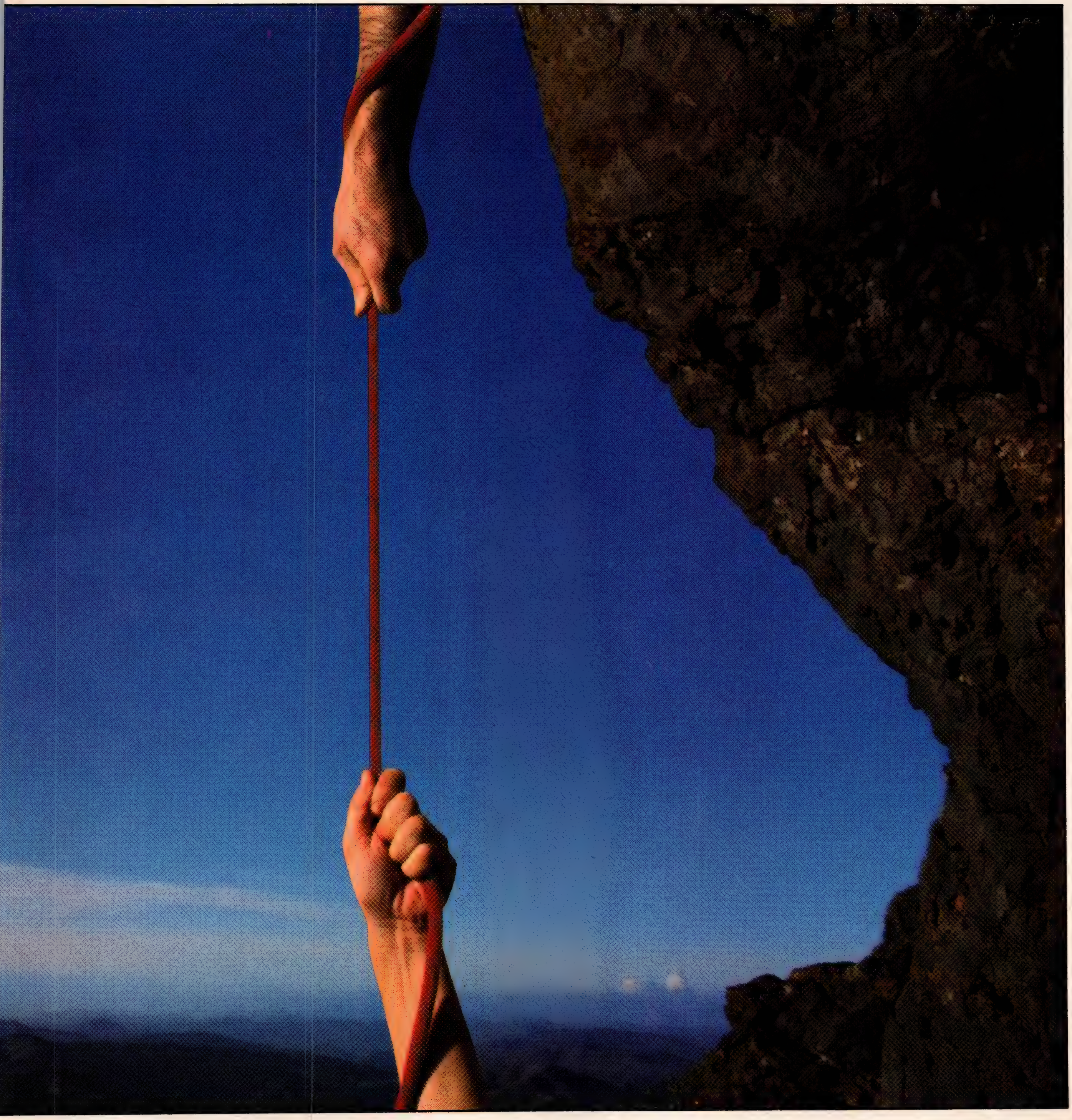

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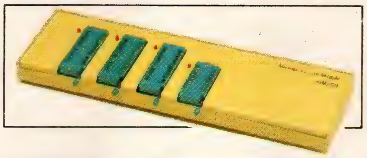

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CIRCLE NO 16

NEWS BREAKS

EDITED BY JOAN MORROW

256k-BIT DRAMs FEATURE 60-nSEC RAS ACCESS TIME

Two CMOS 256k-bit dynamic RAMs from Inmos (Colorado Springs, CO, (303) 630-4000) come with RAS access times of 60 to 150 nsec. The IMS 2800 features static column addressing; the IMS 2801 offers enhanced page-mode operation. A row-address capture window of 4 nsec eases system design by relaxing timing constraints on the multiplexed address lines. The 80-nsec versions of the IMS 2800 and IMS 2801 cost $9.30 (1000) and are available four to six weeks ARO. Inmos is also sampling the IMS 2802 and IMS 2804 256k-bit dynamic RAMs, which feature nibble-mode and an extended serial-mode operation, respectively.—Steven H Leibson

VME BUS 32032 BOARD INCLUDES MMU, FPU, AND I/O

Owl Computers Inc (Encinitas, CA, (619) 436-4214) offers a 32032-based VME Bus board to complement a previously announced Multibus I product. The Model 32032V employs a 10-MHz μP; optionally, it includes the 32081 floating-point unit (FPU) and 32082 memory-management unit (MMU). Without the FPU and MMU, the board sells for $2550 (100). The CPU board also provides 128k bytes of EPROM, two serial ports, and two programmable timers. Standard software includes diagnostics, a monitor, and the Exec real-time operating system. The company also offers the NSX-32 cross-development software library for the IBM PC.—Maury Wright

TWO FIRMS INTRODUCE HIGH-SPEED, SUB-μm CMOS STATIC RAMs

Cypress Semiconductor (San Jose, CA, (408) 943-2666) and Performance Semiconductor (Sunnyvale, CA, (408) 734-8200) have introduced high-speed static RAMs fabricated with CMOS processes that permit the formation of memory cells from FETs having feature geometries of only 0.8 μm. Reduced gate capacitance within these submicron FETs yields gate delays of less than a nanosecond, allowing read/write access times below 25 nsec.

Cypress's CY7C150 1k×4-bit static RAM furnishes access times as low as 15 nsec in the commercial version (−15PC) and 25 nsec in the MIL-STD-883 version (−25DMB); these RAMs sell for $29.40 and $65.05 (100), respectively. Both versions are available in either 24-pin DIPs or 28-pin LCCs. Performance Semiconductor offers a higher density part, the P4C188 16k×4-bit static RAM, with an access time of 20 nsec over the commercial temperature range and 25 nsec for MIL-STD-883 operation. Supplied in either a 22-pin DIP or LCC, the part costs $102 in plastic and $127.50 in ceramic (100).—Denny Cormier

TRIO OF ESDI WINCHESTERS SPANS 85M TO 170M BYTES

Evaluation units of Miniscribe's (Longmont, CO, (303) 651-6000) 6000E Series ESDI 5¼-in. Winchester disk drives should be available this month. The three models—the 6085E, the 6128E, and the 6170E—feature unformatted capacities of 85.3M, 128M, and 170.6M bytes, respectively, and cost $1000, $1150, and $1300 (2500), respectively. The drives furnish a 10M-bps transfer rate, selectable hard or soft sectoring, automatic actuator retraction and locking during power down, and a 17W standby-power-dissipation rating. The line supports several ESDI command options including start and stop spindle, track offset (for data recovery), and programmable hard-sector sizing from 162 to 4096 bytes/sector.—Steven H Leibson

DEVELOPMENT SOFTWARE EXECUTES ON G64 TARGET ENVIRONMENT

Gespac Inc (Mesa, AZ, (602) 962-5559) and Genesis Microsystems Corp (Mountain View, CA, (415) 964-9001) provide a hardware/software package for the IBM PC and compatibles that lets you develop software for Intel 8088/8086-based G64 Bus products on your PC and debug the software on the target hardware. The Genescope and Access software packages from Genesis Microsystems operate with the Gespac GESSBS-5, an 8088-based single-board computer that's compatible with the standard G64 Bus. The Access software package lets you edit, compile, and assemble code on the PC and then download the code to your target G64 hardware. After the downloading operation, you can use the Genescope screen-oriented debugger to execute and debug the code on the target board. The companies also plan ports to the GESSBS-8 8088 board and the GESMPU-18 80286 board. The GESSBS-5 board costs $595; the Genescope EPROM kit costs $1495. Access costs $495.—Maury Wright

STANDARD CELLS DOMINATE CICC PRODUCT INTRODUCTIONS

Although the technical sessions at the Custom Integrated Circuits Conference (CICC) covered a full range of custom-IC technologies, new product announcements centered on standard-cell ICs. At the conference, which was held last month in Rochester, NY, Toshiba America Inc (Sunnyvale, CA) announced the TS22SC family of 2-μm standard cells, which includes ROM macrocells as large as 16k bits and RAM macrocells that contain as much as 4k bits. Also, LSI Logic Corp (Milpitas, CA) introduced large cells called megafunctions that emulate standard products like 2900 bit-slice chips, UARTs, DMA controllers, and multipliers.

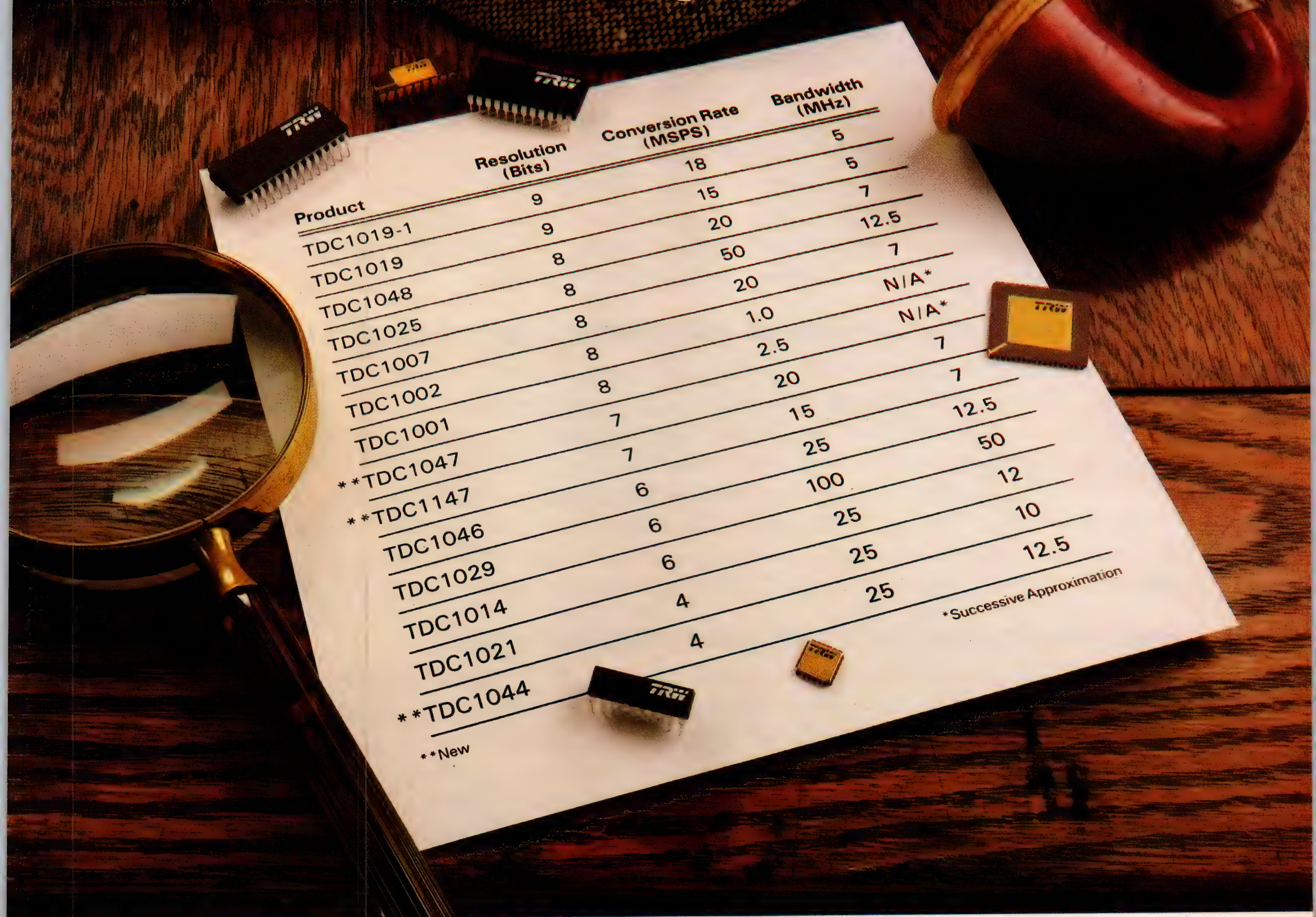
Prominent among the introductions were the CMOS and bipolar capabilities exhibited by VTC Inc's (Minneapolis, MN) VL5000 standard-cell library. It incorporates multipliers, memories, register files, and bit-slice processors, all implemented in a 1-μm CMOS technology. The company claims 575-psec gate delays typ and integration levels as high as 20,000 gates. In addition, VTC announced that it has adapted its VL2000 bipolar standard-cell library for use with IBM PC/AT-based Personal Engineer software from Computervision (Bedford, MA), allowing you to design ICs with 440-psec typ gate delays on a workstation costing between $20,000 and $35,000.—David Smith

STD CONTROLLER CARD FEATURES MULTITASKING BASIC

The $595 880B multifunction CPU card for the STD Bus from Octagon Systems Corp (Westminster, CO, (303) 426-8540) features an 8088 μP, two serial ports, a 16-bit parallel port, five 8-bit timer/counters, an interrupt controller, and a multitasking RoBasic language in ROM. RoBasic is a Basic-compatible language with additional, specialized statements for low-level I/O control. For example, RoBasic has TACH and FREQ statements for measuring the period and frequency of a periodic waveform in 100-μsec increments, a PULSE statement for measuring pulse width, and various statements for converting from hexadecimal, binary, and BCD data formats.

RoBasic can also run multiple tasks concurrently using a 16-entry, circular task queue for scheduling task execution. You can add and delete RoBasic tasks programmably, and you can tie RoBasic software routines to hardware interrupts. Once you have developed a program, you can burn it into EPROM with the RoBasic STORE command using Octagon's 870 STD EPROM programmer card.—Steven H Leibson

There's more here than meets the eye.



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NEWS BREAKS: INTERNATIONAL

BY PETER HAROLD

DSP IC PERFORMS AT 80M FIXED-POINT OPERATIONS/SEC

Recognizing that the majority of digital-signal-processing algorithms can be implemented in the form of a transversal filter, Inmos Ltd (Bristol, UK, TLX 444723) has developed the IMS-A100—a cascadable digital transversal filter IC that contains 32 multiply and accumulate stages on one chip. The internal architecture suits the device to finite-impulse-response filter applications, discrete Fourier transform computations, and similar applications. Each stage operates on 16-bit data, with coefficients of 4, 8, 12, or 16 bits, and the entire array of 32 stages has a cycle time of 400 nsec—equivalent to performing 80 million fixed-point operations per second. You can cascade several devices to construct longer transversal filters. The device is packaged in an 84-pin pin-grid array and costs approximately $500.

DUAL-PORT STATIC RAM FEATURES ON-CHIP ARBITRATION LOGIC

The HM65231 2k×8-bit CMOS dual-port static RAM from Matra Harris (Nantes, France, TLX 711930) has one port with separate address and data buses and a second port with a multiplexed address/data bus, providing a convenient means of communicating between multiplexed and nonmultiplexed μPs or system buses. On-chip arbitration logic operates in three programmable modes, which allows you to use the device between μPs with or without wait-state capabilities, or to switch between the ports under software control. Interrupt outputs and internal flag registers indicate message availability in the RAM. The RAM sells for approximately $19.30 (100).

ELECTRONIC DISK PROVIDES 200M-BYTE CAPACITY

The CCS-95 electronic disk from Compcontrol (Eindhoven, The Netherlands, TLX 51603) eliminates the head-positioning and disk-rotation delays associated with mechanical disk assemblies; it's suitable for use in multiuser computers and real-time data-acquisition systems. Based on a rack of VME Bus memory cards, the CCS-95 has a maximum capacity of 200M bytes. It operates over a 1.5M-byte/sec SCSI interface and occupies eight SCSI bus addresses—six for the unit's 36M-byte memory banks, one for an address controller, and one for a tape or optical disk backup device. The company will customize the SCSI interface to match exactly your computer's existing hard-disk-controller requirements. The electronic disk costs approximately $250,000.

INTERFACE BRIDGES GAP BETWEEN VME AND MULTIBUS I SYSTEMS

Continuing its policy of porting Intel processors and associated application software into the VME Bus domain, High Technology Electronics Ltd (Southampton, UK, TLX 477465) is introducing the HVME-BUSAD—an interface adapter that links Multibus I and VME Bus systems via as much as 6 ft of ribbon cable. Selling for approximately £1500, the interface maps the Multibus system into a 16M-byte VME Bus address map, with the VME Bus arbitration logic handling bus requests from masters on either the VME or Multibus side of the link.

HIGH-FREQUENCY SCOPE FEATURES INFRARED REMOTE CONTROL

You can control the $6500 PM3296 350-MHz oscilloscope from Philips Test & Measurement (Eindhoven, The Netherlands, TLX 51573), from a handheld infrared remote-control unit. This feature allows simple hands-off operation when direct access to the oscilloscope is inconvenient or dangerous. As many as 25 (and optionally 75) complete instrument settings are made via the instrument's front panel or IEEE-488 interface and stored in nonvolatile memory. The infrared control unit then allows you to recall individual setups or to sequence through them.

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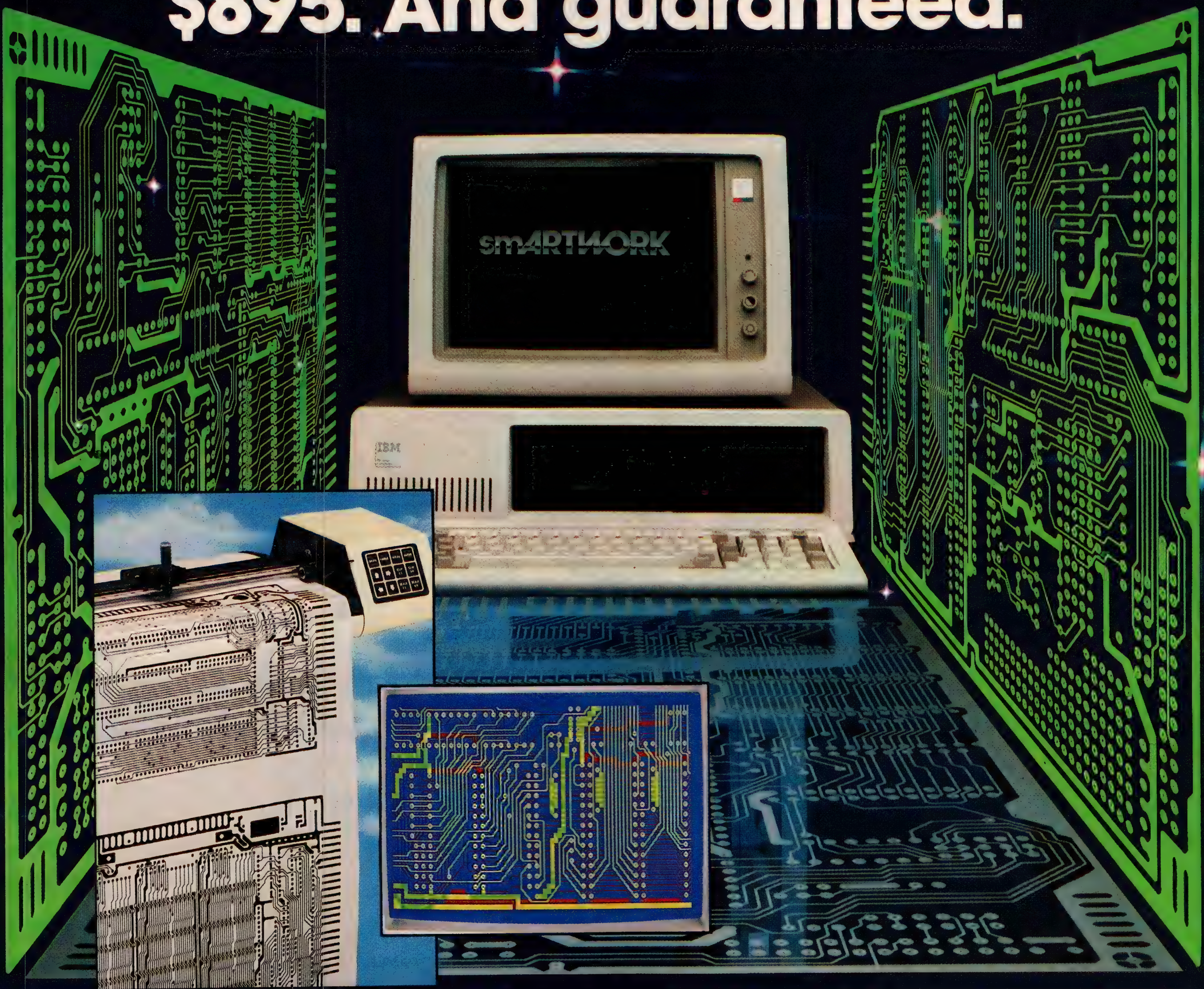

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CIRCLE NO 17

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from $11.95 (1-49)

one-piece design defies rough handling

Check these features:

✓ Each unit undergoes high-impact shock test
✓ Available from 1 to 40 dB
✓ DC to 1500 MHz
✓ Unexcelled temperature stability, .002 dB/°C
✓ 2W max. input power (SMA is 0.5W)
✓ BNC, SMA, N and TNC models
✓ Immediate delivery, 1-yr. guarantee

NEW!
Precision 50-ohm terminations... only $6.95 (1-24)
DC to 2 GHz, 0.25W power rating, VSWR less than 1.1
BNC (model BTRM-50), TNC (model TTRM-50)
SMA (model STRM-50), N (model NTRM-50)

*Freq. (MHz)	Atten. Tol. (Typ.)	Atten. Change, (Typ.) over Freq. Range		VSWR (Max.)	
		DC–1000	1000–1500	DC–1000 MHz	1000–1500 MHz
DC-1500 MHz	±0.3	0.6	0.8	1.3	1.5

*DC–1000 MHz (all 75 ohm or 30 dB models) DC-500 MHz (all 40 dB models)

MODEL AVAILABILITY
Model no. = a series suffix and dash number of attenuation.
Example: CAT-3 is CAT series, 3 dB attenuation.
■ denotes 75 ohms; add −75 to model no.
● denotes 50 ohms

ATTEN	SAT (SMA)	CAT (BNC)	NAT (N)	TAT (TNC)
1	●	●	●	●
2	●	●	●	●
3	●	●■	●	●
4	●	●	●	●
5	●	●	●	●
6	●	●■	●	●
7	●	●	●	●
8	●	●	●	●
9	●	●	●	●
10	●	●■	●	●
12	●	●	●	●
15	●	●■	●	●
20	●	●■	●	●
30	●	●	●	●
40	●	●	●	●

PRICING (1-49 qty.): CAT (BNC)..$11.95, SAT (SMA)..$14.95
TAT (TNC)..$12.95, NAT (N)..$15.95

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setting higher standards

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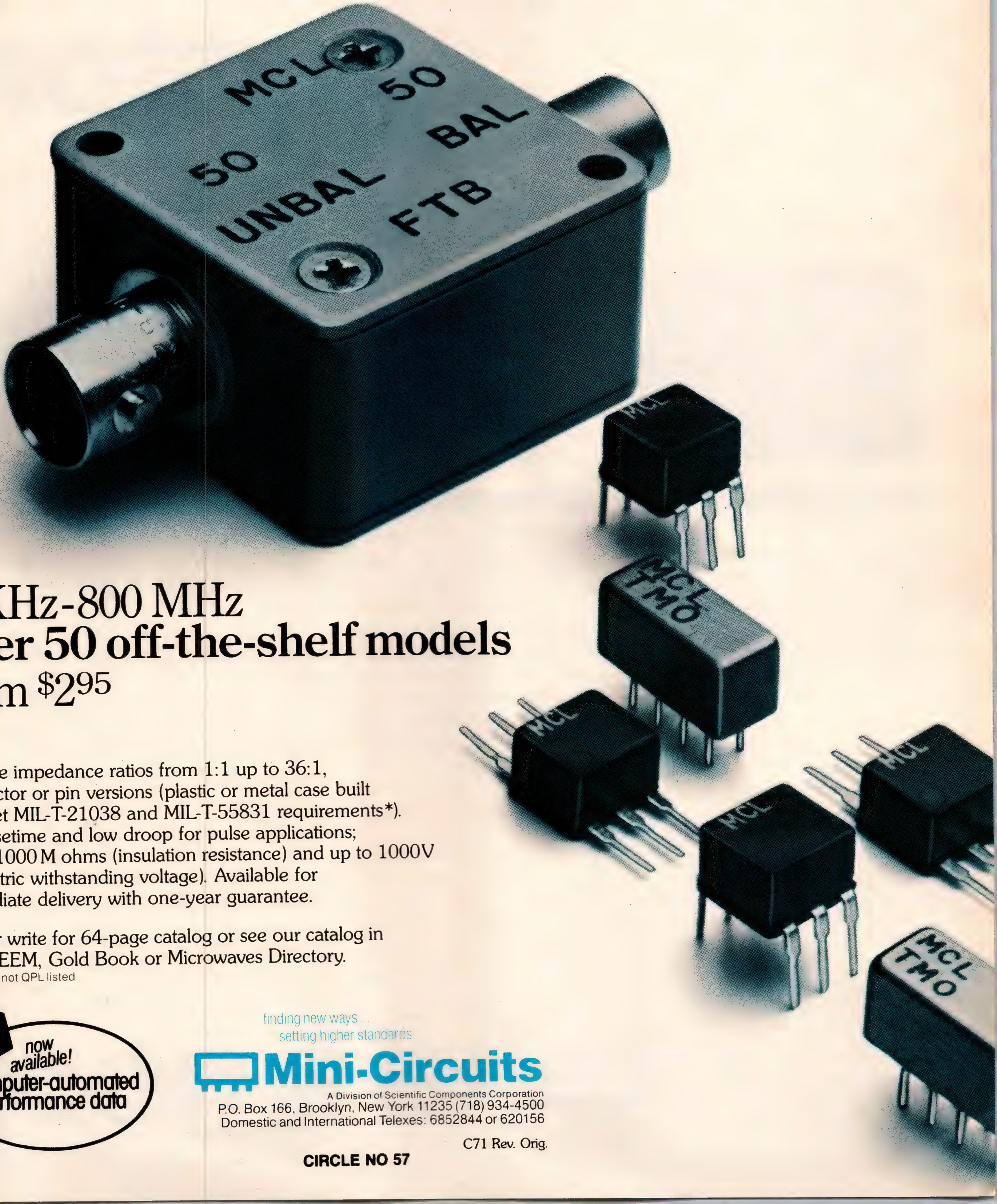
C 92 REV. B

CIRCLE NO 18

RF transformers



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from $2.95

Choose impedance ratios from 1:1 up to 36:1, connector or pin versions (plastic or metal case built to meet MIL-T-21038 and MIL-T-55831 requirements*). Fast risetime and low droop for pulse applications; up to 1000 M ohms (insulation resistance) and up to 1000V (dielectric withstanding voltage). Available for immediate delivery with one-year guarantee.

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*units are not QPL listed

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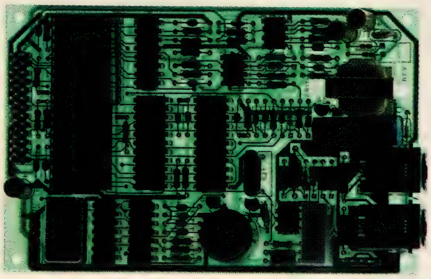
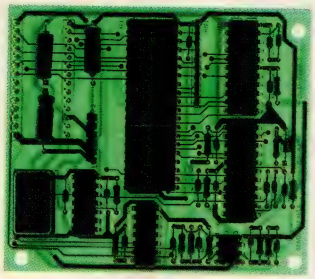
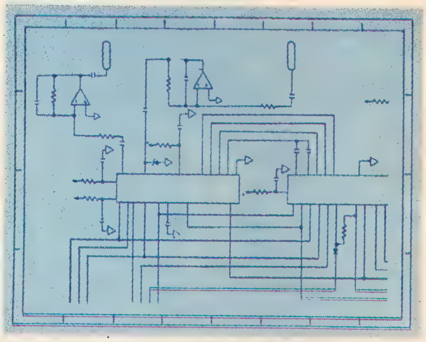
C71 Rev. Orig.

CIRCLE NO 57

When you positively custom







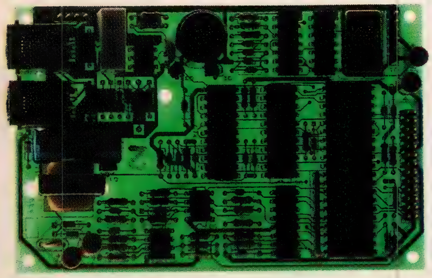
Reliability is your obvious first requirement in this vital link between your product and the outside world. At Ven-Tel—with 12 years experience and millions of modems designed and shipped—we don't take reliability for granted...*so you can.*

Compatibility with industry standards. All Ven-Tel modems utilize the industry standard "AT" command set, guaranteeing compatibility with virtually all types of software. And every Ven-Tel custom modem is fully compatible with our complete line of standard desktop and PC internal modems. We also meet Bell 212A and CCITT V.22bis standards in speeds up to 2400 baud.

Quick Turnaround is more than a phrase to us. We've built a reputation for meeting product deadlines among some of the nation's largest and most demanding manufacturers. From start to finish in as little as 90 days, Ven-Tel can help you get your product to market quickly. You can even begin development using our standard modules while your design is being finalized.

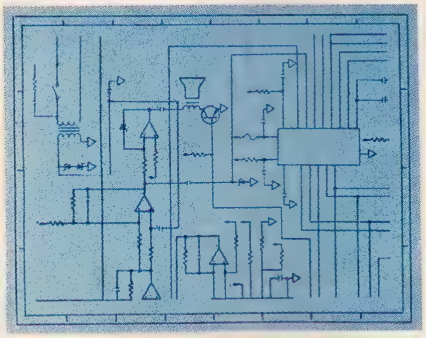
take a good

absolutely, need reliable modems...



Customizing

your modem is your choice. From our standard off-the-shelf boards, to complete custom design, to licensing our proprietary CMOS chip design (for quantities in excess of 100,000 annually), we guarantee the right modem solution based on your deadline, design and volume requirements. Custom hardware configurations and firmware give you maximum freedom for integrating the modem into your overall product design.



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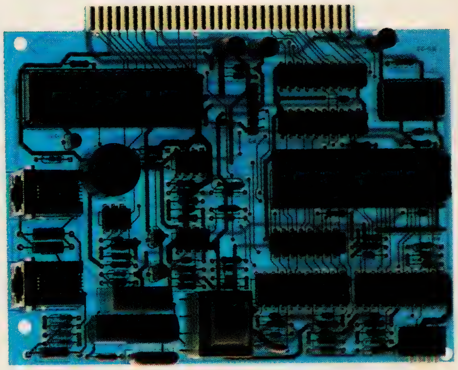
is an important requirement in applications like credit check terminals, portable computers and trouble monitors. Ven-Tel modem density is state-of-the-art to provide excellent "real estate" value, with complete auto-dial/auto-answer, AT compatible, 212A modems—in as little as 12 square inches. With power requirements as low as 500mW.



Competitive Pricing

makes the Ven-Tel custom modem package one definitely worth looking into. For quotations based on your modem specs or a discussion with our experienced OEM sales engineers, call **800/538-5121 (outside California). In California, call 408/727-5721.** Or contact us for our custom modem brochure:
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CIRCLE NO 19

NO ONE LIKES

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TO WAIT !

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Or, if you think that 16 bit will do it for you, get your hands on our brand-new CPU-5 family with "NO WAIT STATE" performance at 12.5 and 16.67 MHz into 128 KByte of local RAM and Floating Point support. Yes, 68000 at 16 MHz.

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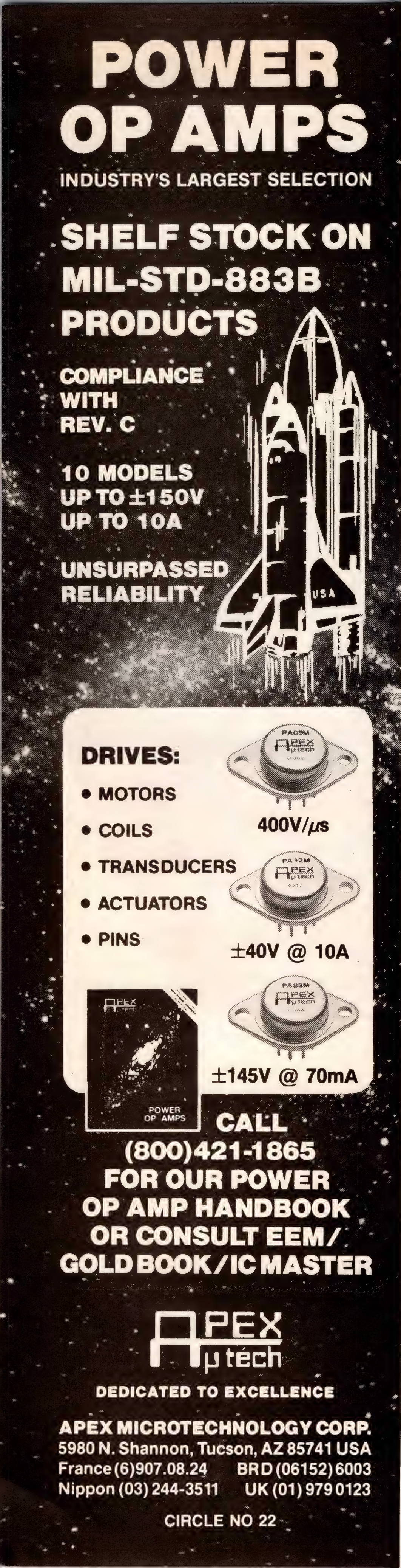


SIGNALS & NOISE

DoD will abrogate right to free speech

Dear Editor:
Deborah Asbrand's article "Recent Department of Defense restrictions target open technical conferences" (EDN, March 20, pg 311) is frightening. I am always dismayed when I hear of people so anxious to give away what is their birthright that they are even willing to assist in the process.

Apart from the foolish people described in the article, the article itself is frightening. What it presents is a balanced set of arguments about destroying our right to free speech. How could a proposal like that be presented in such a detached, balanced, and fair way? Where were the calls to defend our rights? Why is the "minor point" about free speech missing completely from the editorial?

It's not as if we aren't equipped with laws governing secret data; people are prosecuted every day for violating such laws. If the government wants to stop its citizens from giving ideas away, it simply has to classify them as secret. Even if it can't classify the ideas because it doesn't know about them beforehand, our government, with its clumsy attempts at censorship, has no reason to destroy our constitutional right to free speech.

Sincerely yours,
James Brown
Del Mar, CA

(Ed Note: We appreciate Mr Brown's observation that Ms Asbrand's article is a "detached, balanced, and fair" presentation of the issue. We'd like to clarify that the article is not an editorial. Like any article that appears in Professional Issues, this article was intended to present all points of view in the matter so that readers may judge it for themselves.)

Comm industry wants free use of airspace

Dear Editor:
Regarding the editorial "Don't legislate radio security," (EDN, April 3, pg 45), I heartily agree with Jon Titus's views on communication security. The subject has been making me boil. The communication industry wants to deny the public access to its transmissions, yet it wants to use the airspace virtually free, as a public trust.

In essence, members of the industry use my airspace to transmit their signals to make money, but they want to deny me free use of the same airspace. Maybe we should be able to charge fees for the use of the airspace over our property.

To be facetious, who knows what evil lurks in the supersaturated transmissions impinging on me! A study may be advisable to determine whether or not there's a correlation between cancer and other illnesses and immersion in electromagnetic radiation from all sources. Stranger things have happened.

Sincerely yours,
George Schaffer
Rolling Hills Estates, CA

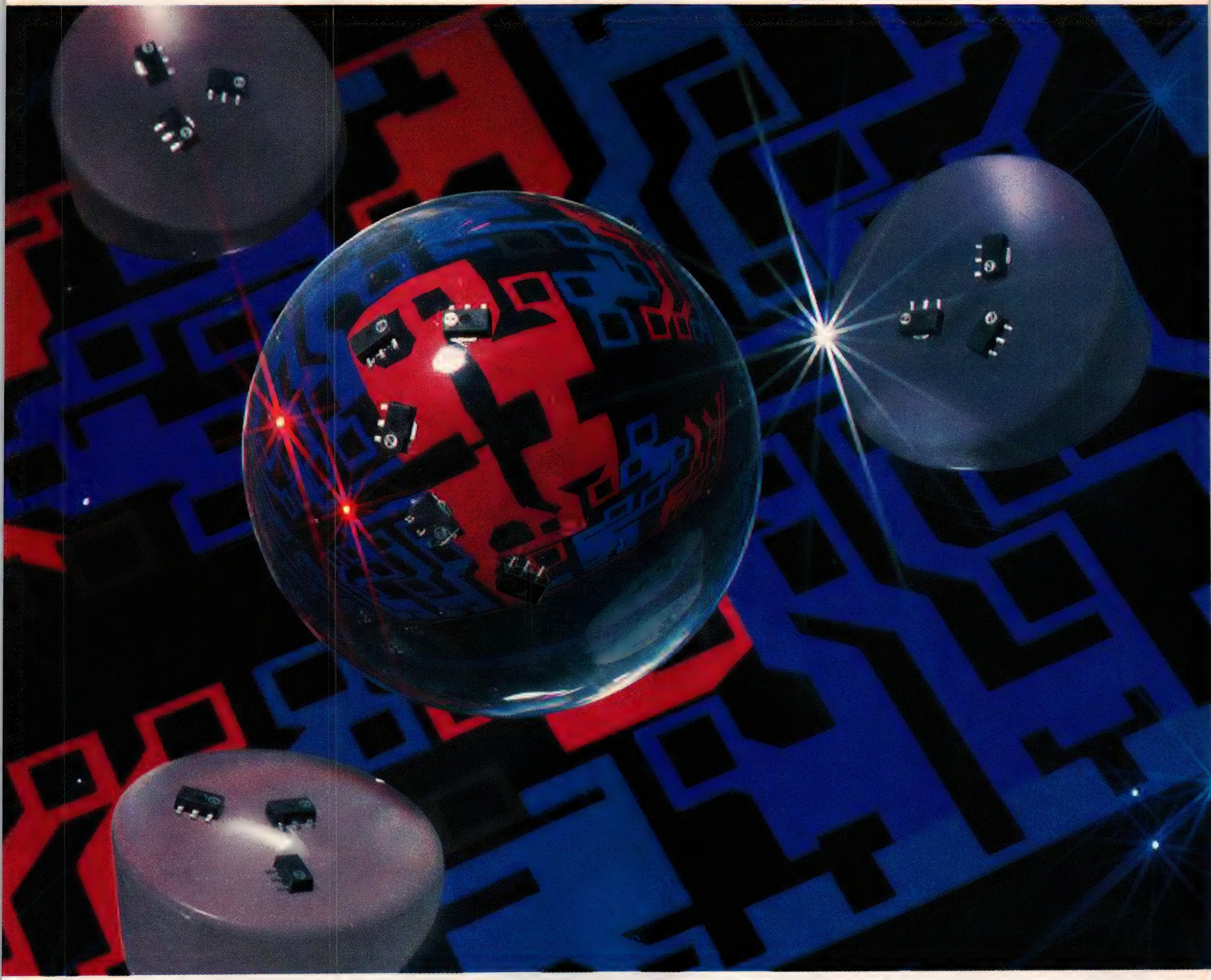
Oops!

In the article "Feed analog signals to IBM PC-compatible personal computers" (EDN, April 17, pg 153), the photos of authors Doug Grant and Scott Wurcer (pg 168) were inadvertently transposed. We apologize for the error.

WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

SENSORS ON-BOARD.



4SH-4166

SPRAGUE MAKES HALL EFFECT ICs FOR SURFACE-MOUNT.

Sprague is the *first* U.S. semiconductor manufacturer to offer all the advantages of solid-state, magnetically activated switches and sensors in SOT-89/TO-243AA plastic packages for surface mounting. Series 3000 Hall Effect digital switches are TTL compatible with a supply voltage range of 4.5 to 24 V. Series 3500 linear sensors track small changes in magnetic field strength and are used to detect the proximity of ferrous metals or the current carried by a cable. All of our linear circuits have an emitter-follower output stage. Both series are available with long leads for through-board mounting. Whether your requirements for surface-mount devices are driven by application or cost, Sprague is committed to supporting you.

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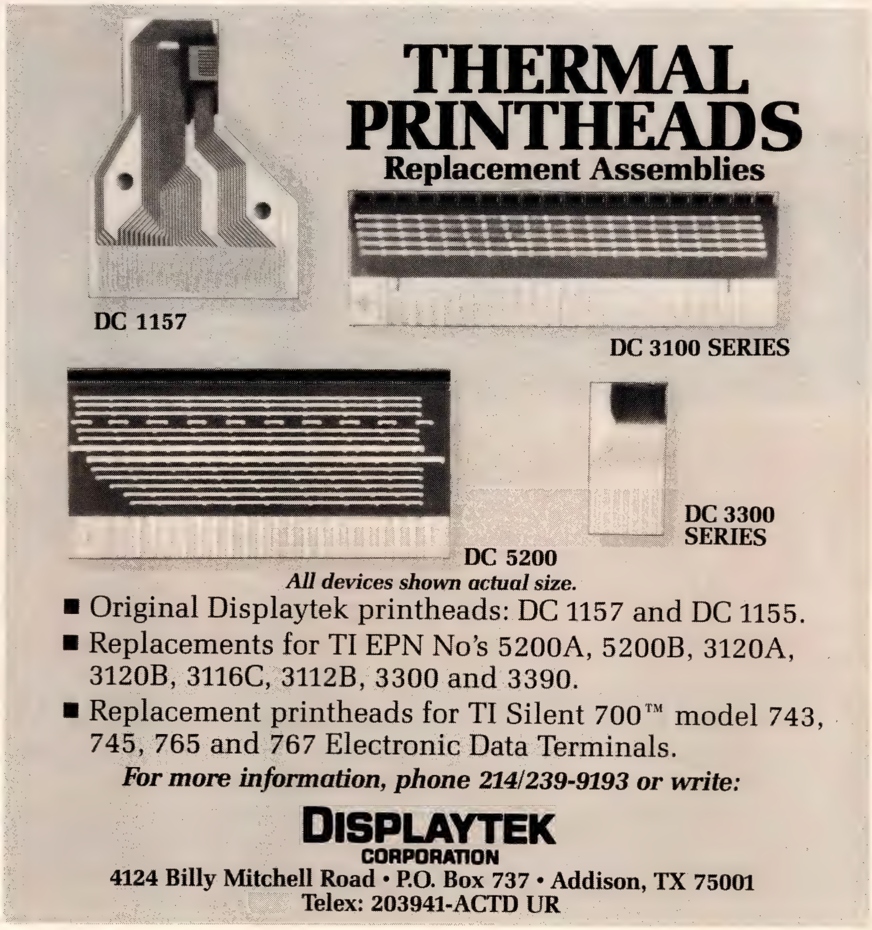

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Oscilloscope or Display Device	TEK CAMERAS High Writing Rate	General Purpose	Low Cost
Tek 5000 Series			
5100 Series Non-storage: 5110, 5112, D10, D12, 577/D1, 5116		C-59A	C-4 OPT02, C-5C, C-7, C-7 OPT01
5100 Series Storage: 5111, 5111A, 5113, 5115, D11, D13, D15, 577/D2		C-59A	C-4 OPT02, C-5C, C-7, C-7 OPT01
5400 Series Non-storage: 5403/D40, 5440, 5444, D40		C-59A	C-4 OPT02, C-5C, C-7, C-7 OPT01
5400 Series Storage: 5403/D41, 5441, D41	C-51	C-53	C-4 OPT02, C-5C, C-7, C-7 OPT01
5223		C-59A	C-4 OPT02, C-5C, C-7, C-7 OPT01
Tek 7000 Series			
8 cm x 10 cm Display i.e.; 7104, 7503, R7103, 7504, 7514, 7613N, 7623, 7633, 7704(A), 7834, 7844, 7854, R7903, 7904, 7904A, T922R	C-51 C-31B OPT01	C-53 C-30B OPT01	C-4 OPT02 C-5C, C-5C OPT01, C-7, C-7 OPT01
Large Screen Display i.e.; 7403, 7603, 7603N		C-59A	C-4 OPT02 C-5C, C-5C OPT01, C-7, C-7 OPT01
Tek Portables			
Older with 0.8 cm Graticule i.e.; 422, 453, 454, 485, 491	C-31B	C-30B	C-4
Newer w/1 cm Graticule i.e.; 2235 Option 01; 2400 Series, 455, 464, 465, 465B, 465M, 466, 468, R468, 475, 475A, 432, 434, 442	C-31B OPT01	C-30B OPT01	C-4 C-7 OPT02, C-7 OPT03, C-5C OPT02, C-5C OPT04
1 cm Nonilluminated Graticule, 2213(A), 2215(A), 2220, 2230, 2235(L), 2236			C-7 OPT02, C-5C OPT04
¼ inch Graticule i.e.; 305, 314, 326, 335, 336, 1501, 1502		C-30B OPT01	C-4 OPT03
TM 500 i.e.; SC 502, SC 503, SC 504		C-30B OPT01	
Nonilluminated Graticule 2335, 2336(YA), 2337			C-7 OPT02, C-5C OPT04
Tek Display Monitors			
8 cm x 10 cm i.e.; 601, 602, 605, 606, 606B, 607		C-59A	C-4 OPT02 C-5C, C-7, C-7 OPT01
Large Screen 10 x 12 cm i.e.; 603, 604, 608, 620, 624, 634		C-59A	C-4 OPT02 C-5C, C-7, C-7 OPT01
Tek Older 5 Inch Round			
502, 503, 504, 515, 516, 519, 530 & 540, 550/580 Series, 575	C-51	C-53	C-59A
Tek Older 5 Inch Rectangular			
560 Series i.e.; 561, 564, 567, 568		C-53	C-59A
Tek TV Products			
380, 381	C-30B OPT01		
520, 520A, 521, 521A, 522A		C-59A	
1480C		C-53	C-59A
528A, 1420, 1421, 1422, 1424		C-59A	C-4 OPT02 C-5C, C-7, C-7 OPT01
529		C-53	
1710B, 1711B, 1740, 1741, 1742, 1750		C-30B OPT01	C-4 C-7 OPT02, C-7 OPT03, C-5C OPT02, C-5C OPT04

Oscilloscope or Display Device	TEK CAMERAS High Writing Rate	General Purpose	Low Cost
Tek Spectrum Analyzers			
491		C-30B	
492, 492P, 494, 494P, 496, 496P, 2755/P		C-59A	C-4 OPT02 C-5C, C-7, C-7 OPT01
Tek Miscellaneous			
576, 5030, 5031		Only C-59(A)	
OF 150, OF 151, OF 152, OF 235, TDR			C-4 OPT02 C-5C, C-7, C-7 OPT01
1240			C-4 OPT11
T900 Series, excluding T922R, (see 7000 Series)			C-5C OPT03, C-7 OPT04
Hewlett Packard*			
1715A/22B/ 25A/26A/27A 1740A/41A/42A 43A/44A			C-4 C-5C OPT02*** C-5C OPT04***
1745A/46A (9.5 x 12 cm)			C-4 OPT02
5″ rectangular CRTs: 140B/T, 141B/T 180/C/D, 181/AR/T/TR, 183/191A, 193A, 1600A, 3580A** 3720A/21A/ 90A, 3702B/12A 8412A/B 853A W/8557A/ 8558B/8559A 8754A			C-4 OPT02 C-5C (Hand held), C-5C OPT01 (Hand held), C-7 (Hand held), C-7 OPT01 (Hand held)
1200A/B, 1201B, 1205B, 1220B, 1222B			C-5C (Hand held), C-7 (Hand held)
*HP instruments without illuminated graticules which are non-storage require a C-5C or C-7 with flash. **Note: C-50 Series will not fit. ***Bezel is a little too wide for hood, i.e. a tight fit.			
1332A/33/35A 36A/36S/ 40A/45A/ 46A/47A 1980A/B/S 3582A/85A 5181A, 5420A/23A 8505A/A504 A565A/66A/66S 68A/68S 8756A/S		C-59A	C-4 OPT02 C-5C, C-5C OPT01, C-7, C-7 OPT01
5″ round CRTs: 140A, 141A, 8414B/8413		C-59A	
182T, 8755S			C-4 OPT02

Oscilloscope or Display Device	TEK CAMERAS High Writing Rate	General Purpose	Low Cost
B & K			
1466A/76A/ 77/79B 1500/22/25/ 35A/40/ 60/66A/ 70/70A 90/90A 96	C-31B OPT01	C30B OPT01	C-4 C-5C OPT02, C-5C OPT04
Gould*			
OS250, 260 OS1000A OS1400, 1403, 1420 OS3000/A, 3001/A, 3300B, 3350, 3351 OS4000, 4020/22/24 4030, 4035/135 4040/42/43/44			C-5C OPT04
OS4500			C-4 OPT02
*Gould instruments which do not have illuminated graticules and are non-storage require C-5C with flash.			
Hameg			
HM203*/204/ 208/605/ 705/808			C-4 OPT02
*Requires C-5C or C-7 with flash.			
Hitachi			
V-134/151F*/ 152F*/202F/ 203K/211*/ 212*/222/ 223/302F*/ 352F/353F/ 422/423/ 650F/1050F 1070/1100A VC-6015/6041			C-4 OPT02 C-5C, C-5C OPT01
*Requires C-5C with flash.			
Iwatsu			
SS5321/ 5710C/D SS5702/05/06 5711/C/D 5802		C-30B OPT01	C-4 C-5C OPT02, C-5C OPT04
SS8120		C-59A	C-4 OPT02
TS8123		C-59A	C-5C, C-7, C-7 OPT01
Kikusui			
COS5020/21/ 40/41/42/ 60/60A COS5100 COS5513/16ST/ 20/30A/31 COS5630/ 50/50E COS6100/6150 DSS6520/20A/21/22	C-31B OPT01	C-30B OPT01	C-4 C-5C OPT02, C-5 OPT04
Leader			
LB051M/MV/ 513A/514A 514AP/516/ 517/518/ 522/523/524/ 524L/525L 5825/5860A			C-4 C-5C OPT02, C-5C OPT04
Philips			
PM3207/11/12/ 15/17/19 3206/32/ 33/34/62/ 63/63X 3264/66/67 3305/3310/ C/3311/C 3315 3540/42/43			C-4 C-5C OPT02 (Hand held), C-5C OPT04 (Hand held)
Takeda Riken			
TR4122B			C-4 OPT02 C-5C

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Order your camera through the National Marketing Center and for a limited time get free film worth up to $60! Film types available from Tek include: 612, 667, 669, 691, 331 and 339.

Shown above: the Tek C-53 camera on "swing away" bezel mount. The C-53 is just one of a complete line of CRT cameras from low-cost handheld models to those designed to photograph single shot events. Video terminal cameras are also available.

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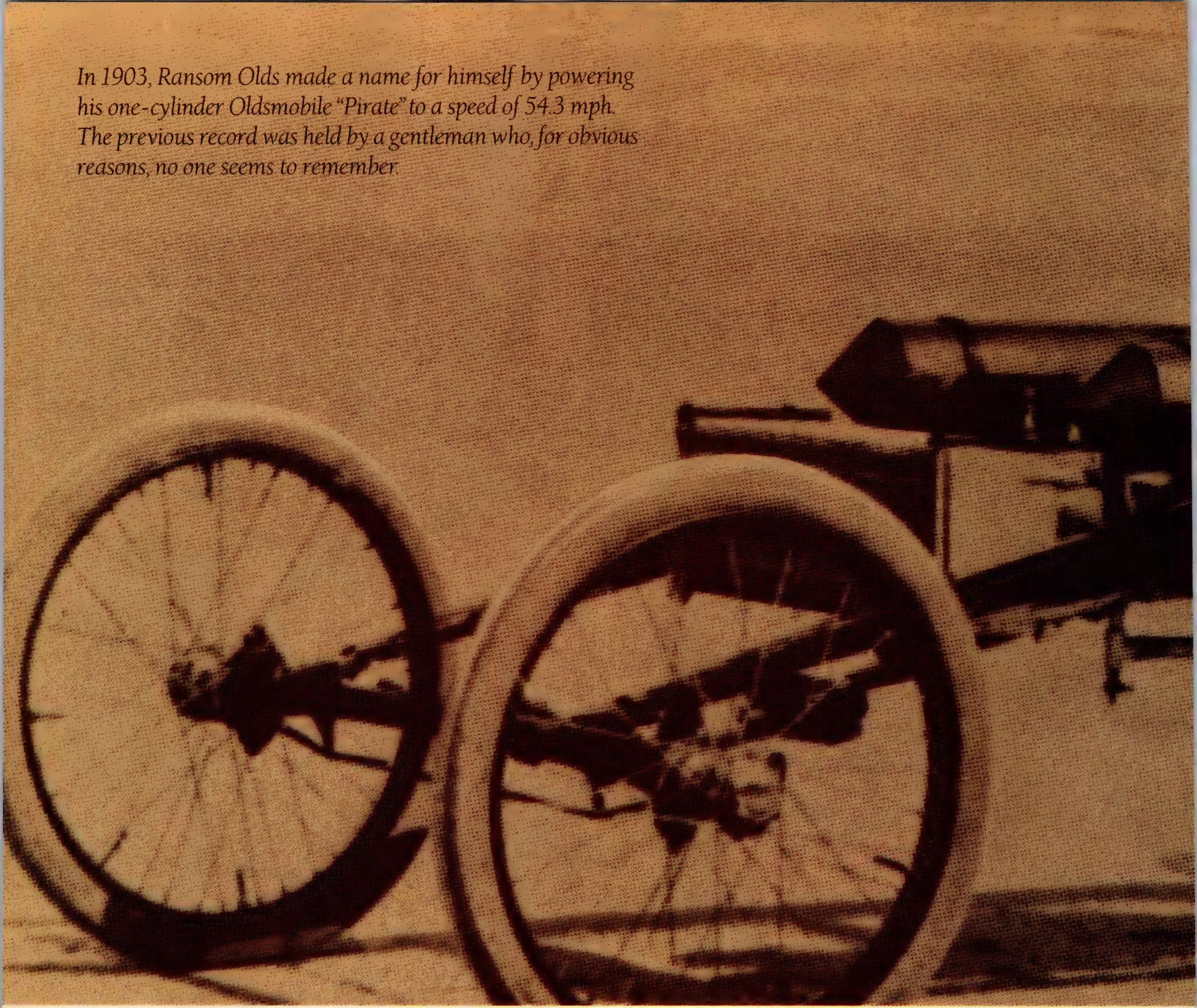
CIRCLE NO 26

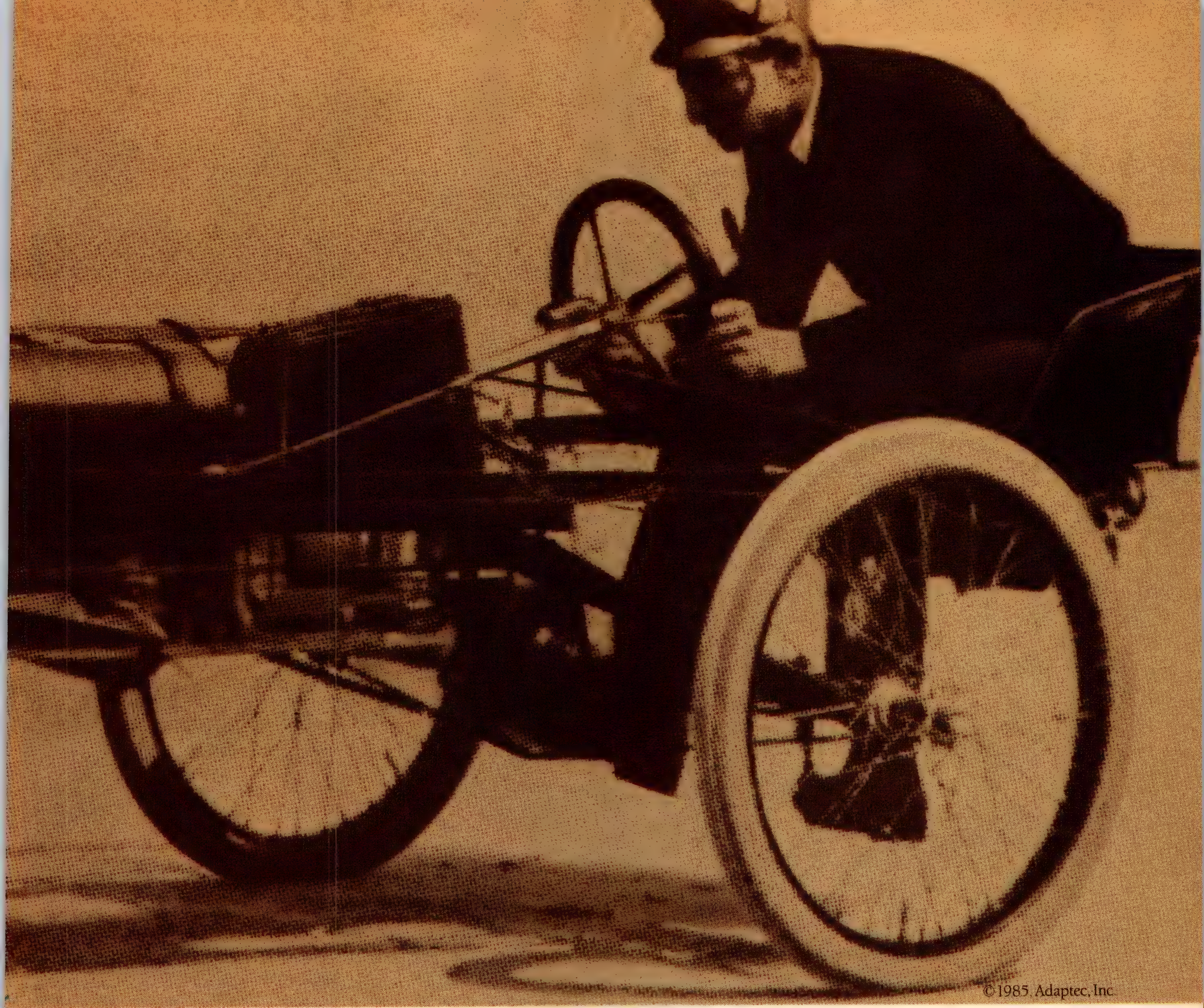


YOU'RE EITHER FAST OR YOU'RE FORGOTTEN.

Engineers have always had a love affair with speed. Whatever they make, they want to make it go faster.

In the computer business, that's especially true. However, building a faster system is not always as simple as adding a faster processor or the fastest drives. It may be some little thing you never think of.

Say, for instance, an I/O controller. And that's what Adaptec is all about.

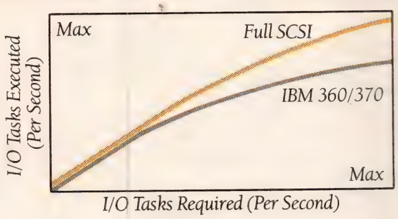


MAINFRAME I/O IN A MICRO.

Adaptec's I/O controllers use an I/O interface derived from mainframes, known as SCSI.

It's our full implementation of SCSI—an industry first—that gives our boards their high performance features.

Like Multithreaded I/O, 1:1 Interleave, Sector Level Defect Skipping and Disconnect/Reconnect.



Adaptec's SCSI controllers can actually outperform a mainframe.

Put them all together and your system can run concurrent I/O tasks with increased data transfer rates and faster access to data.

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CIRCLE NO 27

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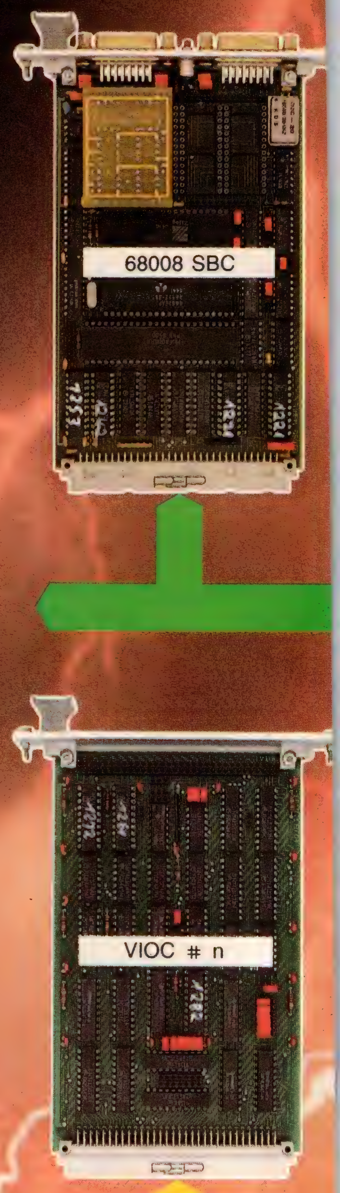
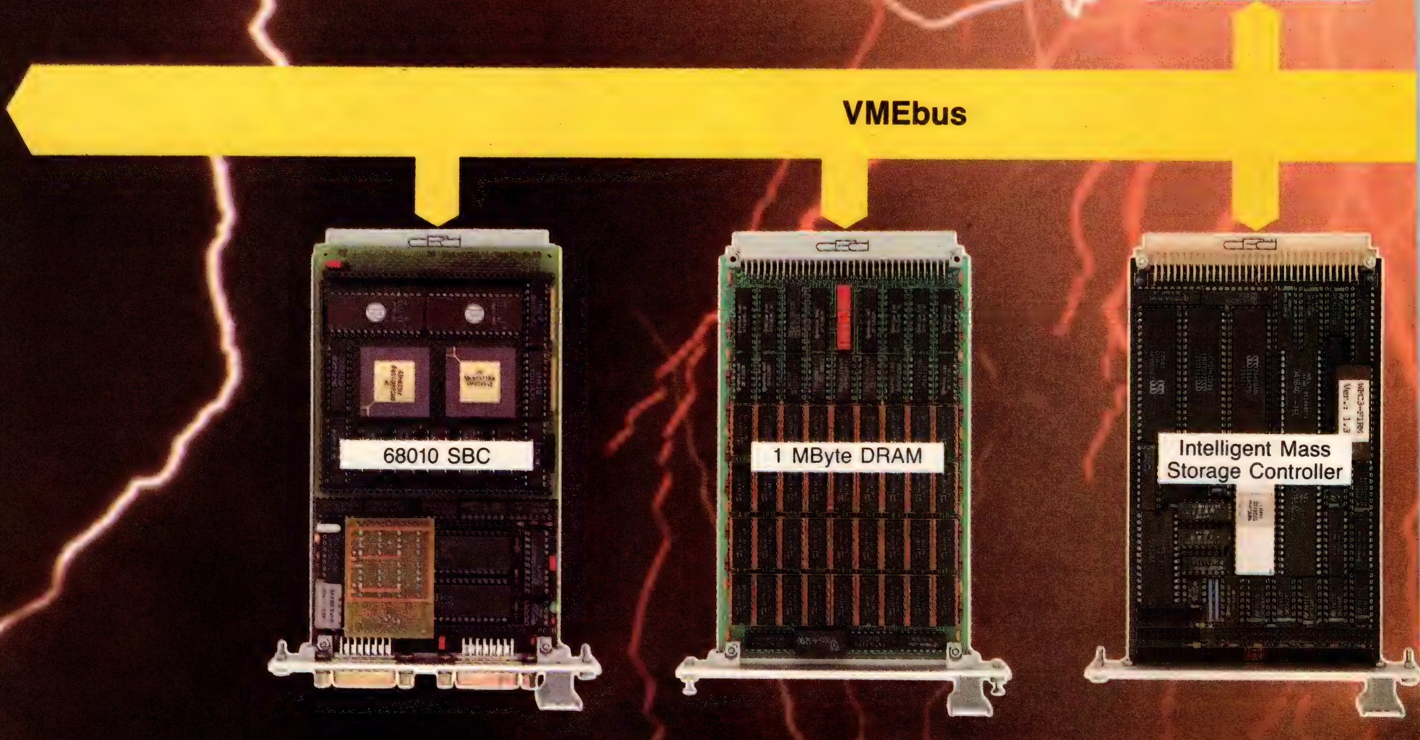
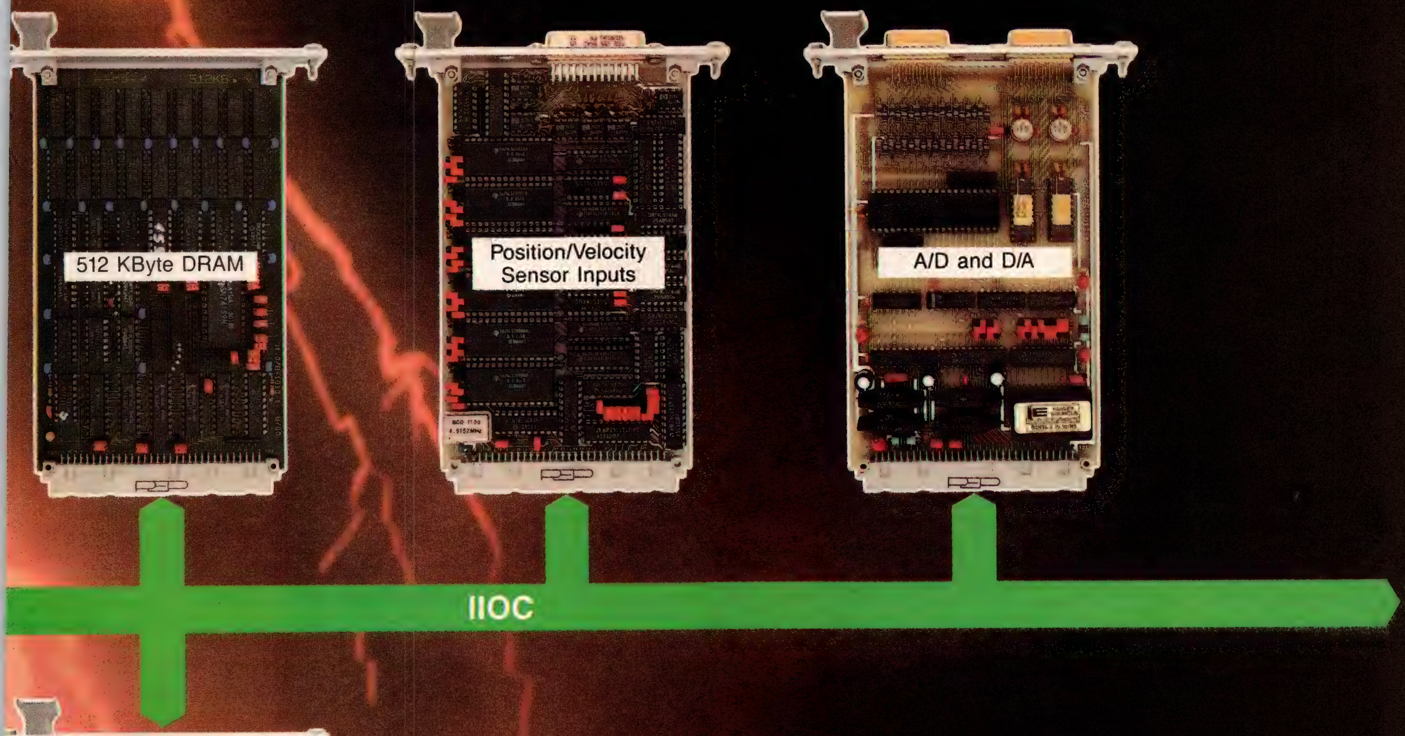
How we tailor VMEbus solutions to your industrial applications



VMEbus and Intelligent I/O Channel...

With the VMEbus finding overwhelming acceptance worldwide, PEP is now enhancing VMEbus versatility with the Intelligent I/O Channel (IIOC). The IIOC provides you with lower cost interface modules typically used in industrial applications. It can also be furnished with its own CPU which can execute tasks locally, offloading the VMEbus master CPU. The IIOC can also be used stand alone. With or without CPU, the IIOC is accessed transparently (as a 64 Kbyte memory mapped space), eliminating the need for complex multiprocessor operating systems. Furthermore, there is no limitation in the number of IIOC's on the VMEbus other than for physical space.





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	Series	Contact Type	Contact Form	Contact Rating	Coil Volts (VDC)	Coil Res. Ω±10% @20°C	Pull In Volts (VDC)	Drop Out Volts (VDC)	Model Number	Fig.
MINI	SE	DRY	1B	10W 100V .5A	5 12 24	500 500 2000	3.8 8.0 16.0	0.5 1.0 2.0	SE1B05AXJ SE1B12AXJ SE1B24AXJ	1.
				10W 100V .5A	5 12 24	500 500 2000	3.5 8.0 16.0	0.5 1.0 2.0	SE1B05AXP SE1B12AXP SE1B24AXP	2.
	SG		1A	10W 200V .5A	5 12 24	500 500 2000	3.5 8.0 16.0	0.5 1.0 2.0	SG1A05AXJD SG1A12AXJD SG1A24AXJD	3.
				10W 200V .5A	5 12 24	500 500 2000	3.5 8.0 16.0	0.5 1.0 2.0	SG1A05AWJ SG1A12AWJ SG1A24AWJ	3.
THIN	DH			10W 100V .5A	5 12 24	500 1000 2000	3.8 8.0 16.0	0.5 1.0 2.0	DH1A05BW DH1A12BW DH1A24BW	4.

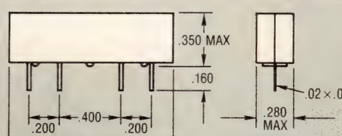

FIGURE 1.

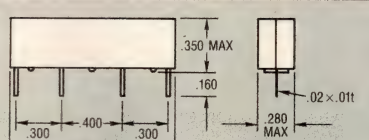

FIGURE 2.

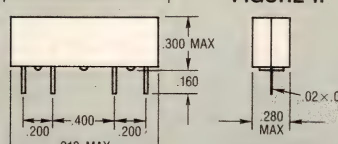

FIGURE 3.

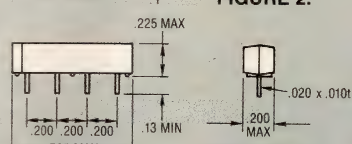

FIGURE 4.

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CALENDAR

IEEE International Conference on Communications '86, Toronto, Canada. IEEE Communications Society, 1450 Don Mills Rd, Don Mills, Ontario, Canada, M3B 2X7. (416) 445-6641. June 22 to 25.

Society of Women Engineers National Convention, Hartford, CT. Society of Women Engineers, 345 E 47th St, New York, NY 10017. (212) 705-7855. June 22 to 29.

Effective Use of In-Circuit and Functional Testing (short course), Milwaukee, WI. Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N 6th St, Milwaukee, WI 53203. (414) 224-3952. June 23 to 25.

ATE East, Boston, MA. Morgan-Grampian Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. June 23 to 26.

EFOC/LAN '86 (European Fiber Optic Communications and Local Area Networks Exposition), Amsterdam, Holland. In US, contact Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134; (617) 232-3111. In Europe, contact IGI Europe, c/o AKM, Box 6, 4005 Basel, Switzerland; 061-50-88-66. June 23 to 27.

AutoCAD Expo '86, Chicago, IL. Peggy Steffens, Autodesk, 2320 Marinship Way, Sausalito, CA 94965. (415) 332-2344, x703. June 24 to 26.

International Aerospace and Ground Conference on Lightning and Static Electricity, Dayton, OH. Larry Walko, US Air Force, AFWAL/FIESL, Wright-Patterson Air Force Base, OH 45433. (513) 257-7718. June 24 to 26.

Surface-Mount Design/Manufacturing (short course), Boston, MA. AWI, 558 Oakmead Parkway,

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CALENDAR

Sunnyvale, CA 94086. (408) 720-8860. June 26 to 27.

ACM/IEEE Design Automation Conference, Las Vegas, NV. MP Associates, 7366 Old Mill, Suite 101, Boulder, CO 80301. (303) 530-4333. June 29 to July 2.

Semicon/Osaka, Osaka, Japan. Semiconductor Equipment and Materials Institute, 625 Ellis St, Suite 212, Mountain View, CA 94043. (415) 964-5111. July 1 to 3.

IEEE Compass '86 (Computer Assurance—Systems Integrity: Process Security and Safety), Washington, DC. Albert Friend, IEEE Compass, Box 3815, Gaithersburg, MD 20878. July 7 to 11.

Effective Implementation of Surface-Mount Technology (short course), Milwaukee, WI. Center for Continuing Engineering Education, College of Engineering and Applied Science, 929 N 6th St, Milwaukee, WI 53203. (414) 224-3952. July 14 to 16.

Modern Power Conversion Design Techniques (short course), Chicago, IL. E/J Bloom Associates, 115 Duran Dr, San Rafael, CA 94903. (415) 492-8443. July 14 to 18.

23rd Annual Conference on Nuclear and Space Radiation Effects, Providence, RI. David Bushmire, Publicity Chairman, Sandia National Laboratories, Organization 2151, Albuquerque, NM 87185. (505) 844-6572. July 21 to 23.

Inter-Noise '86 (International Conference on Noise Control Engineering), Cambridge, MA. Gayle Fitzgerald, Office of Special Events, Massachusetts Institute of Technology, Room 7-111, Cambridge, MA 02139. July 21 to 23.

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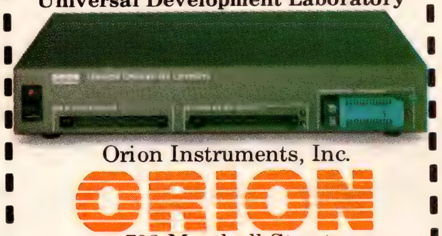

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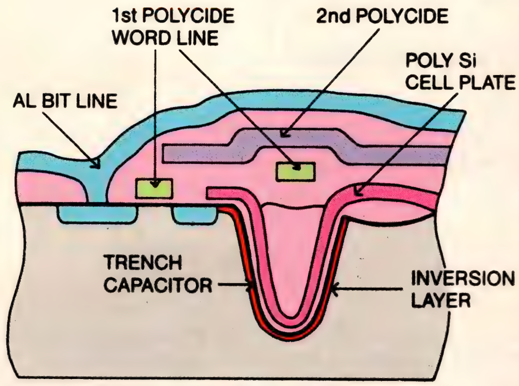
PHILIPS

Entrenched 1 Megabit in 4 Megabit

That the future belongs to large capacity memory components is not hard to visualize, but it takes real vision and know-how to produce a solution today that meets the demands of tomorrow. So it's no coincidence that NEC's 1 Megabit DRAM features technological advances identified with the 4 Megabit realm. The NMOS chip is based on double level polycide technology and uses a 1.0 μ design rule. And of course, there is the revolutionary trench capacitor design that puts the chip way out in front of products using the conventional planar capacitor method.

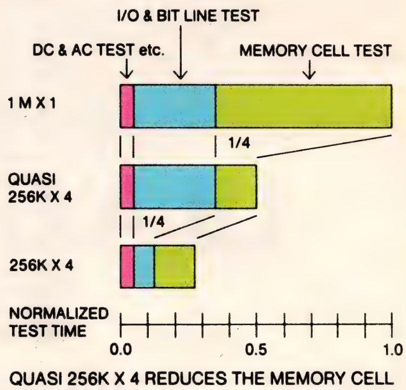


MEMORY CELL WITH A TRENCH CAPACITOR

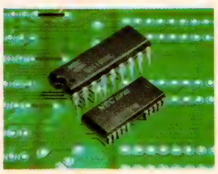
The result is a 1 Megabit DRAM of extremely compact dimensions. In fact, the die size is less than 50 sq mm in cross-section. The tiny size permits a meaningful choice in space-saving packaging – either a 300-mil wide 18-pin plastic DIP, or a SOJ housing appropriate

in the Future
t DRAM
Technology!

for surface-mounting techniques. Not to mention increased product reliability thanks to radically improved alpha particle resistivity, which results in a soft error rate matching that of a 256 Kbit DRAM. The 1 Megabit DRAM is organized as 1,048,576 X 1 bit and operates off a single 5V power supply. Functions include nibble or page mode, CAS-before -RAS refresh, and sophisticated test circuitry. NEC have integrated a 4-bit wide test mode that cuts total testing time by up to half. This keeps testing costs down, but maintains a high level of product reliability – essential factors in volume production of large capacity memory chips.



QUASI 256K X 4 REDUCES THE MEMORY CELL TEST TIME TO 1/4.



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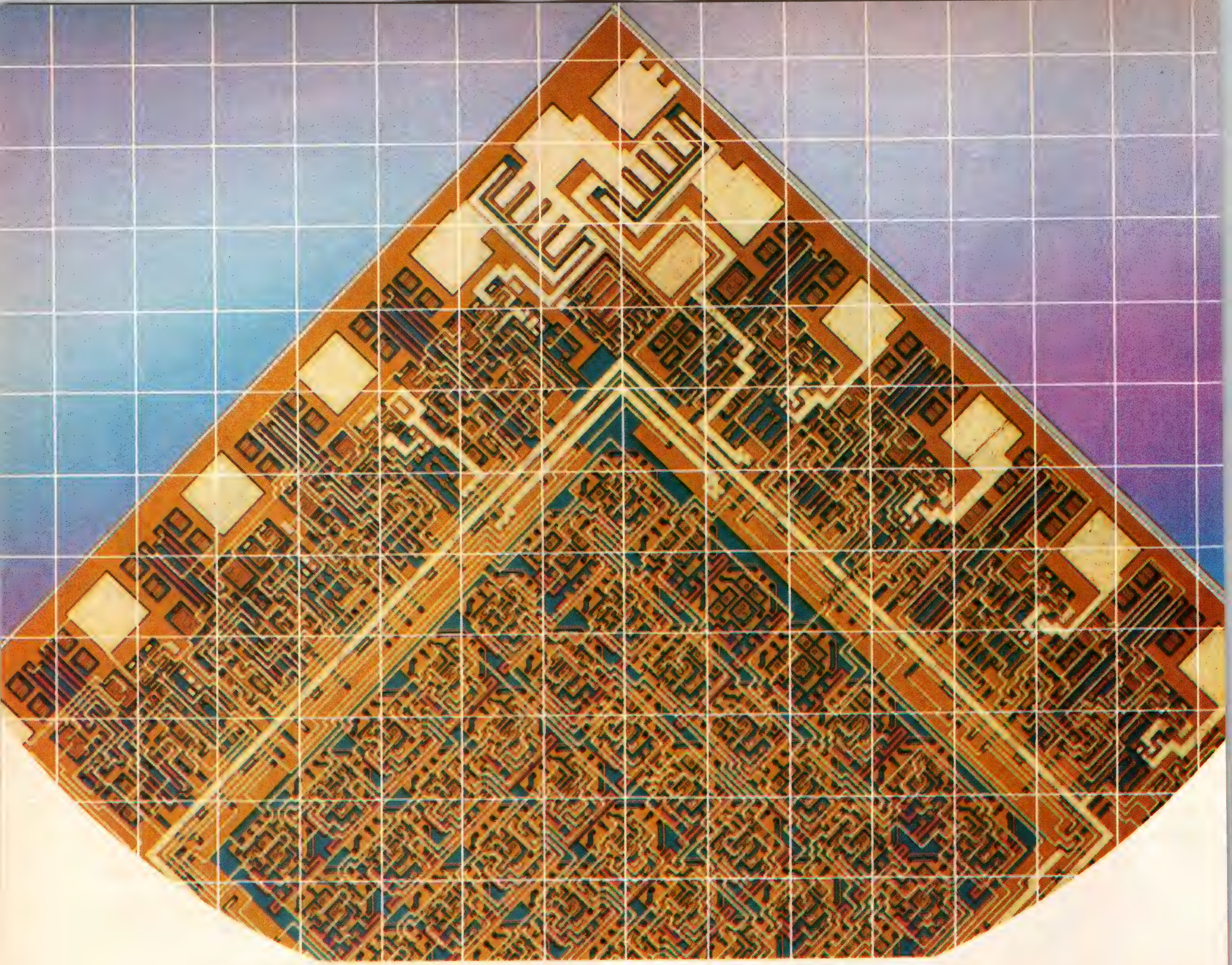

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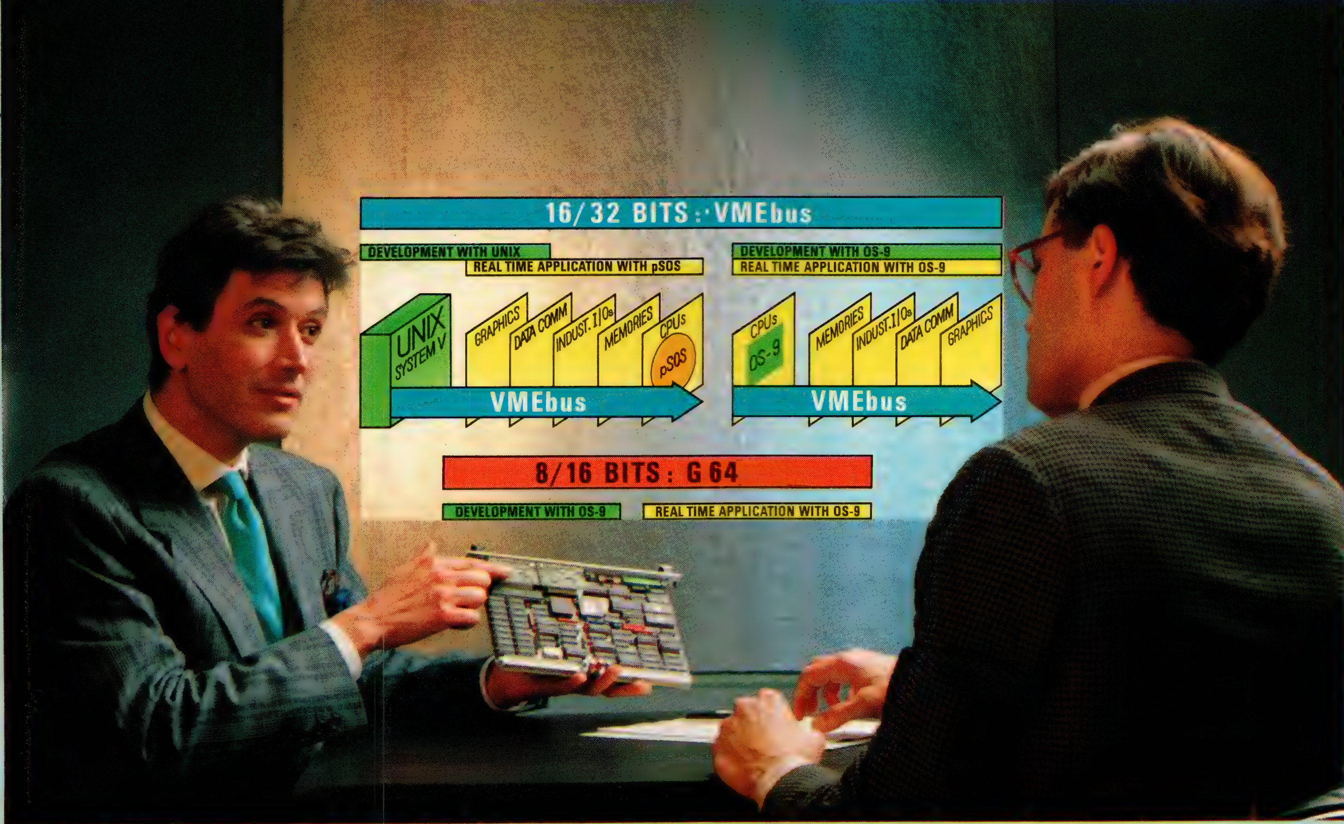
CIRCLE NO 37



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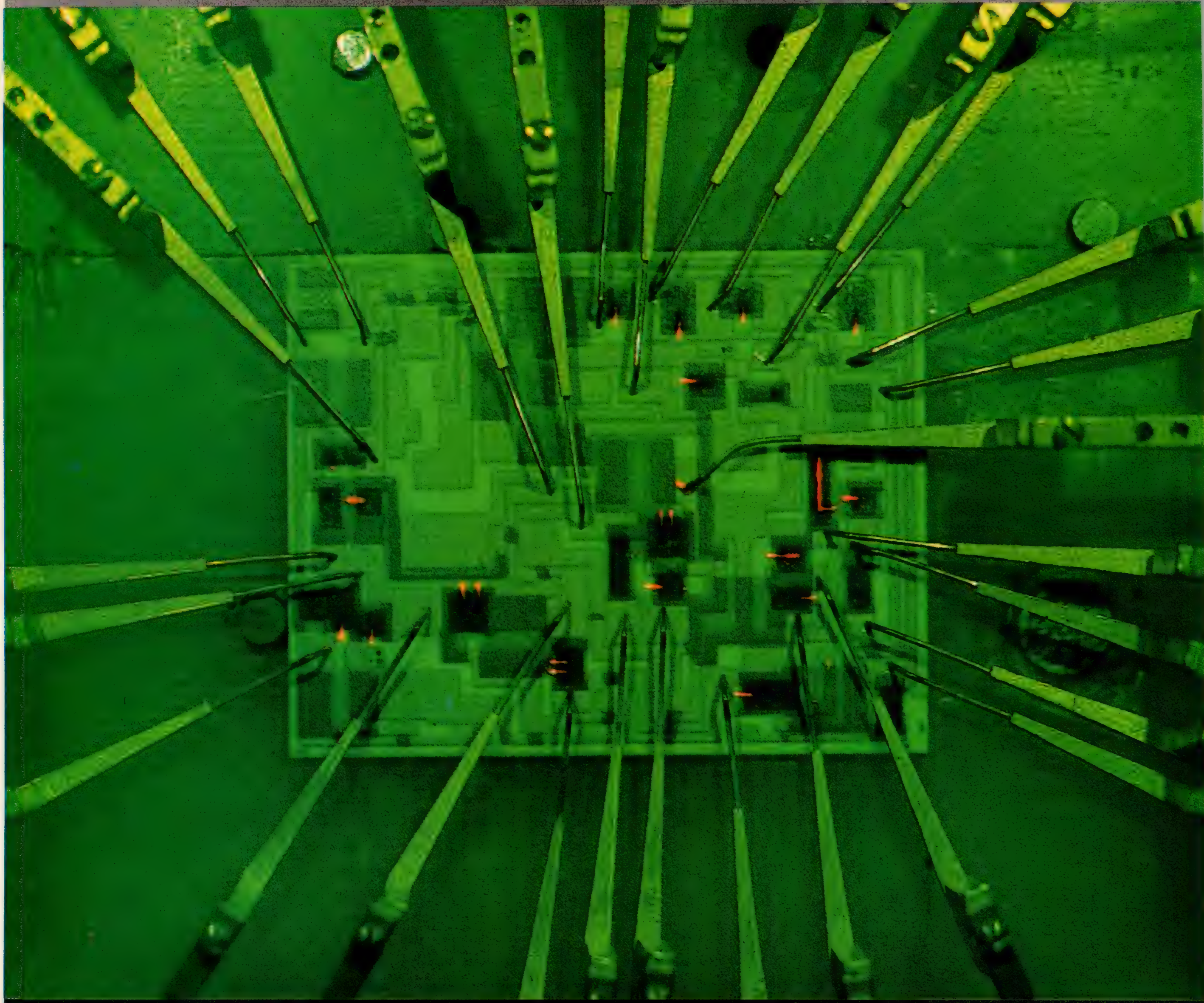
CIRCLE NO 38



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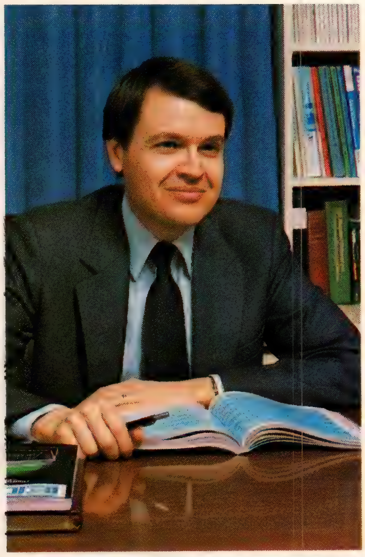
CIRCLE NO 205

Engineers, managers, and the money stream



Let me tell you about the Money Stream Theory of Charles D Small. Small, an engineer for some 48 years and the father of EDN Associate Editor Charles H Small, developed the theory many years ago and has espoused it ever since. It makes a lot of sense to me, so I thought I'd pass it on.

Briefly, the theory is this: A money stream runs through every company; money comes in (revenue), and money goes out (expenditures). The closer you are to the incoming flow, the higher your salary, position, and prestige are likely to be. The closer you are to the outgoing flow, however—or worse yet, the farther you are from the stream entirely—the bleaker your prospects.

A vice president of marketing or sales, for example, stands a good chance of advancing to president, but a vice president of engineering does not. Similarly, a sales manager has greater potential than an engineering manager, and a sales engineer has more opportunities than a design engineer. The designer can be just as smart, work just as hard, and be just as valuable (or more valuable) to the company, and yet the sales engineer is more likely to advance. And it's all due, according to Charles D Small, to the designer's remoteness from the money stream.

Sad to say, Small's theory is true. Sadder yet, the situation it describes is inescapable. Design engineers and managers—unless they draw closer to the money stream by forsaking their chosen professional activity and much of their professional experience—are destined for only moderate financial success and prestige.

Of course, Small's theory applies on a more general scale. Labor unions have tried, with little success, to obtain power for their members, who typically are far from any money stream. Socialism, invented by Karl Marx to advance the working class, has done little to narrow the gap between the moneyless, powerless proletariat and the moneyed, powerful ruling class.

The message for designers and design managers, then, isn't particularly cheerful. From Francis Bacon's lofty statement, in 1597, that knowledge is power, we move to Tennessee Williams's statement, in the twentieth century, that knowledge, money, and power are a cycle. Engineers, despite their vast knowledge, can't complete the cycle to power without gravitating toward the money stream by making career moves that might, in some respects, be ill advised.

Gary Legg

Gary Legg
Editor

WEEK 33

If you hate waiting around crowded registers, AMD's new Am29524 Dual 7-Deep Pipeline Register is for you. It's designed for applications that need ground or data pass-through. So now your input data can fly directly to the output or your output can be all zeroes.

Am29524

Direct flights.

The Am29524 has 14, not 16, registers like the Am29525. But it shares many of the same attributes. With the Am29524 you can dip into the data registers in any order, at any time. You could think of it as a random access register. It's programmed by microcode instructions to hold, shift or load data. Its internal ECL technology gives the Am29524 incredible speed (it has a 21ns propagation delay) and the I/O is three-state TTL compatible.

Need to get rid of some excess baggage like a register and bus buffer? The Am29524 does the work of both. And we packed it all in a 28-pin DIP package.

Flying the Am29524 isn't for just everyone. Only the people who want to travel direct.

CIRCLE NO 48

WEEK 34

AMD wants to put power back where it belongs: In your hands.

We're proud to announce the Am29C821 10-bit CMOS Bus Interface Register. It's a member of the high performance Am29C800 Family: The family that delivers the performance you expect from the bipolar Am29800 Family but with stingy power demands.

Am29C821

Seize power.

The register requires a low power stand-by current of 80 microAmps. But AMD promises that taking power from it won't slow it to molasses. The Am29C821 has a propagation delay of 12ns.

You can also use it in place of, or along with, the Am29800 bipolar counterpart to match your drive and power requirements. Used where an Am29821 provides 48mA drive, the Am29C821 provides 24mA drive.

Get yourself the Am29C821. And then give the leftover power to someone who can really use it.

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CIRCLE NO 87

WEEK 35

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Am29C116

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WEEK 36

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Am29C843

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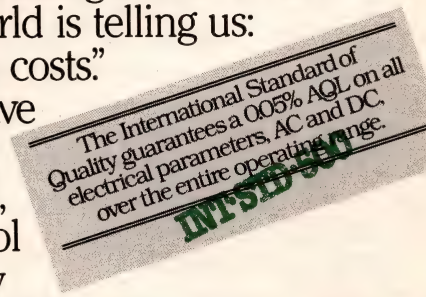

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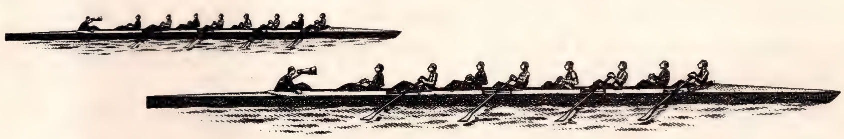

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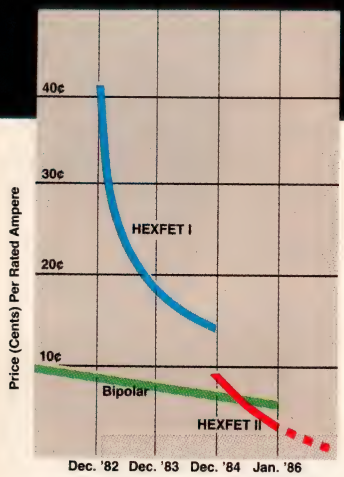

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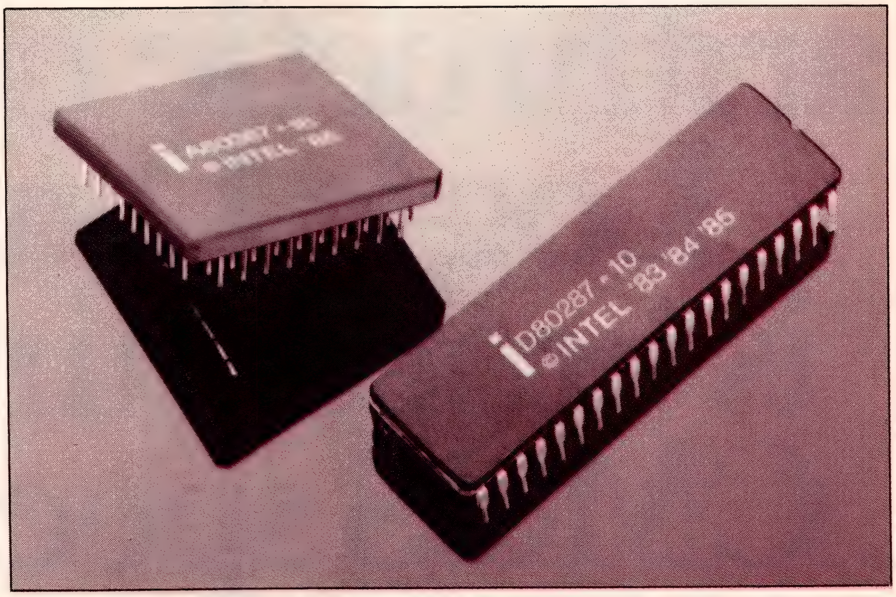
Design precautions ensure the benefits of using floating-point coprocessors

Jon Titus, *Senior Editor*

There's more to accelerating math-intensive software than simply putting a floating-point coprocessor (FPC) chip in your computer design. Because math chips require more software support than do general-purpose peripherals, designing a math chip into a μC system requires caution. Moreover, floating-point-coprocessor chips operate most efficiently within their own μP family. Mixing FPC and CPU chips from different families is a difficult task, and it leaves little flexibility for designers.



Typical floating-point math coprocessor chips *support a range of mathematical functions that offer speed advantages over math software routines. Manufacturers supply chips in PGA and DIP forms.*

You should, however, balance the lack of FPC choices for a given μP against the many useful functions that each family's math chip provides. Highly sophisticated FPC chips include Intel's 80287 for the 8086/80286 family and Motorola's MC68881 for the MC68000/68020 family. These FPCs offer standard arithmetic operations as well as log, exponential, and transcendental functions.

Other FPC chips provide hardware math operations for National's NS32000 and AT&T's WE32100 μP families (see **Table 1**). Texas Instruments is a second source for National's 32000 family and its 32081 math chip. FPCs under development include NEC's μPD72191 math chip for its V Series μPs; the μPD72191 should be available in the third quarter. Following it should be AT&T's WE32206 for its new WE32200 μC family and Intel's 80387 chip for its 80386 CPU chip.

Your choice of an FPC chip depends on either the μP chip you're already using or the type of software you want to run. If your goal is to run math-intensive programs whose instructions take advantage of a particular FPC's capabilities, you should consider choosing the μP and FPC chips as a set, thus determining your computer's CPU and math-processing requirements simultaneously.

If you've already selected a μP chip, it's unlikely that you'll choose an incompatible, nonfamily FPC chip for your computer system, so timing and speed comparisons of different FPC chips are pointless. For example, although your application might take advantage of the MC68881 math chip's features, it's unlikely that you'll design it into an Intel 80286-based computer. Any increase in performance would be offset immediately by the extra software and control logic you'll need to mate the MC68881 with the 80286.

Keep in mind that your math coprocessor's efficiency depends greatly on the software you're running. You'll get a good estimate of processing efficiency by running your software in a computer lacking an FPC and then in an equivalent computer that includes an FPC. For example, Motorola reports that a computer based on a 16.5-MHz MC68020 without an FPC chip runs a Monte Carlo simulation routine in 108 sec. When an MC68881 chip also running at 16.5 MHz replaces the math-processing software, the simulation routine takes 5.7 sec.

Not all applications will run 19 times faster, but it's reasonable to expect an FPC chip to confer a tenfold increase in math-processing speed. However, plugging an FPC chip into your computer doesn't automatically boost the CPU's math-processing speeds. The operating system or control software must include steps that detect the FPC chip, and it must include routines that control the chip's math and data-transfer operations.

Software that includes many com-

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LMU557/558	8 x 8 mixed	60	70	25S557/8
LMU12	12 x 12	65	100	MPY12HJ
LMU13	12 x 12 microprogrammable	65	100	–
LMU16	16 x 16	80	125	MPY16HJ; AM29516
LMU17	16 x 16 microprogrammable	80	125	AM29517
LMU18	16 x 16 32-bit output	80	150	–
MULTIPLIER-ACCUMULATORS				
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LMA1009	12 x 12	65	100	TDC1009
LMA1010	16 x 16	90	100	TDC1010
LMA1043	16 x 16	90	100	TDC1043
PIPELINE REGISTERS				
Part No.	Type	Max. Access Time (ns)	Power (mW)	Equivalent
L29C520/521	4 x 8 bit	22	50	AM29520/521
LPR520/21	4 x 16 bit	22	50	two AM29520/521
MULTIPORT REGISTER FILES				
Part No.	Type	Max. Access Time (ns)	Power (mW)	Equivalent
LRF07	3 independent port, 8 x 8	35	40	–
LRF08	5 independent port, 8 x 8	35	60	–
ARITHMETIC LOGIC UNITS				
Part No.	Type	Min. Cycle Time (ns)	Power (mW)	Equivalent
L429C01	16-bit slice	90	150	Quad 2901 or 2901D
L4C381	16-bit adder/subtractor	34	75	Quad 54/74S381
SPECIAL-FUNCTION CIRCUITS				
Part No.	Type	Performance	Power (mW)	Equivalent
LSH32	32-bit barrel shifter	35 ns prop. delay	60	–
L10C23	64-bit digital correlator	35 MHz data rate	125	TDC1023J

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TABLE 1—FLOATING-POINT MATH COPROCESSOR CHIPS

MANUFACTURER	AT&T	MOTOROLA	INTEL	NATIONAL	NEC
MODEL	WE32106	MC68881	80287	NS32081[1]	μPD72191
μP FAMILY	WE32100	MC68020	80286	NS32000	V-40, V-50
BUS WIDTH	32 BITS	32, 16, OR 8 BITS	16 BITS	16 BITS	8 BITS OR 16 BITS
DATA REGISTERS	4 (80 BITS)	8 (80 BITS)	8 (80 BITS)	8 (32 BITS) OR 4 (64 BITS)	8 (80 BITS)
DATA FORMATS					
INTEGER	•	•	•	•	•
FLOATING POINT	•	•	•	•	•
PACKED BCD	•	•	•		•
MATH OPERATIONS					
+ − × ÷	•	•	•	•	•
LOG/EXP		•			•
TRIG		•	•		•
CONSTANTS[2]		•	•		•
OTHER[3]	•	•	•	•	•
PACKAGE	100-PIN OR 125-PIN PGA	68-PIN PGA	40-PIN DIP	24-PIN DIP	40-PIN DIP
PRICE	$250 (1)	$119 (100) (FOUR TO SIX WEEKS DELIVERY)	$350 (100)	$20 (100)	

NOTES:
1. TEXAS INSTRUMENTS IS A SECOND SOURCE FOR THE 32081 FPC CHIP, $64.70 (100, CERAMIC PACKAGE).
2. CONSTANT VALUES INCLUDE π, e, 0.0, 1.0, $LOG_{10}2$, ETC.
3. OTHER OPERATIONS INVOLVE ROUNDING, TRUNCATING, SQUARE ROOT, SQUARE, ETC.

plex math operations—the Monte Carlo simulation routine, for example—benefits more from an FPC than does software that performs simple, repetitive math operations. Complex math operations written in an interpreted language, such as Basic, benefit only slightly from FPC operations. Although the FPC speeds the math operations, the computer still spends most of its time interpreting the program's Basic commands to determine what math operations to do. As a consequence, you gain only a small increase in performance.

μP makers offer software

To let you take advantage of an FPC chip's math-processing power, the μP manufacturers supply debuggers, assemblers, libraries, and other software packages that directly support their FPC chips. You'll also find C, Fortran, Pascal, Basic, and other compilers that take advantage of FPC math operations. Manufacturers also sell software libraries that simulate their FPC chips. The software traps the coprocessor instructions and emulates the corresponding math operations. Consequently, you can develop, test, and debug your math software without actually running it on a computer that contains an FPC chip. The simulation software can also serve in place of an FPC until your system develops to the point where it can take full advantage of the coprocessor's superior performance.

If the simulation software operates with the standard coprocessor instructions instead of special trap instructions, you can add an FPC chip to the computer system and use it without modifying your math software. Just instruct the software to stop trapping the coprocessor instructions and to pass them to the FPC instead.

In an MC68020-based computer without an MC68881 FPC chip, coprocessor instructions force the CPU into an exception condition. To simulate the MC68881 chip, the exception-processing software decodes the coprocessor's instruction and points to emulation routines that perform the equivalent MC68881 math operations. When you place an MC68881 chip in your computer, the coprocessor instructions no longer cause exception conditions. Instead, the FPC automatically receives its instructions and performs the indicated operations. Motorola provides sample software that shows you how to write the exception-processing routines.

Intel's 80286 μP chip contains two flag bits that let you trap math coprocessor instructions. The CPU's MP flag in its machine-status word reflects the presence or absence of a coprocessor chip. The EM flag lets the CPU know whether you want it to emulate the coprocessor's tasks in software. By setting or clearing the 80286 CPU's MP and EM flags when you run an application program, you can decide whether to use the 80287 or to emu-

late its functions. Intel's iCEL software package provides 80287 emulation routines.

Interrupts replace math codes

Trapping instructions in an 8086/8088 computer system involves additional programming work. When used with 8086/88 systems, Intel's LINK86 program replaces all the 2-byte coprocessor codes in your program with 2-byte interrupt instructions. When the CPU encounters a substitute interrupt instruction, the interrupt vector table points to the proper emulation routine. This instruction-substitution strategy has a drawback, however. An 8086/88 program that traps coprocessor instructions can't automatically switch to coprocessor operation, because the coprocessor instructions have been changed.

AT&T's library of coprocessor-emulation routines operates in WE32100-based computers to simulate WE32106 math-chip operations. Besides standard program-development software, AT&T provides Cobol, C, Fortran-77, Basic, and Pascal compilers that support a WE32106 chip in a WE32100-based computer.

Although software instructions and internal operations vary from one type of FPC chip to another, the chips share one attribute: speed. To take advantage of an FPC's high-speed math operations, μP-system designers tightly couple the FPC and CPU chips, thus minimizing data-transfer and instruction-decoding overhead in both interface circuits and control software. To keep data-transfer times as short as possible, the μP families map the FPC chip's data and control registers into the CPU's register address map. In an MC68020/68881 computer system, the FPC's internal registers appear to the programmer as though they're a part of the CPU.

Although the coprocessor instructions you put in your program appear to control the FPC chip directly, it's the CPU that performs the control operations. The CPU fetches and decodes the math instructions and transfers data to and from the FPC's registers. For example, in an 80286-based computer, 1- to 4-byte escape (ESC) instructions in the program control an 80287 coprocessor chip's operations. When the CPU decodes an ESC op code, the FPC must perform the action encoded in the ESC instruction. The FPC doesn't control the computer's bus: Only the host CPU fetches and executes instructions.

When the 80286 encounters an ESC instruction, it checks the 80287 to be sure the FPC isn't processing data. When the FPC is ready, the CPU reads data from the computer's memory so the FPC can accept it from the data bus. The FPC cannot transfer data directly to or from memory on its own. In fact, all of the FPC chips rely on the host CPU for data- or instruction-transfer operations.

Instructions identify FPCs

Motorola's MC68881 FPC chip also relies on the CPU to fetch instructions, but unlike the 80287, the chip doesn't duplicate the CPU's internal instruction-decoding activity. Instead, the MC68881 responds to F-line codes that come from the CPU and identify as many as eight coprocessors and control their operations. The MC68881's F-line codes vary from one to as many as eight words in length, and they contain instructions, values, and addresses.

The AT&T WE32106 chip operates in a similar manner. The CPU initiates FPC transactions by broadcasting a command word that identifies one coprocessor chip. The identified coprocessor reads a command word and performs the associated task. If the command requires an operand from the computer's memory, the CPU performs the necessary memory-read operations. The FPC monitors the data bus and reads the proper number of 32-bit values. The FPC then transmits a synchronizing signal to the CPU to coordinate bus-transfer operations.

Data formats are standard

Although the FPC chips each have their own commands and instruction formats, the data formats they support are standard. Most FPC chips support three numeric formats—integer, floating point, and binary-coded decimal (BCD)—as specified in the IEEE Task P754 Revision 10.0 standard

For more information . . .

For more information on the math coprocessor chips described in this article, contact the following manufacturers directly or circle the appropriate number on the Information Retrieval Service card.

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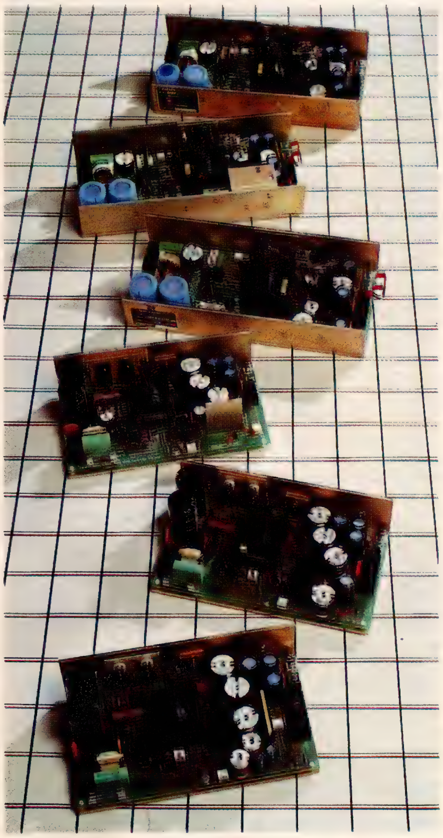

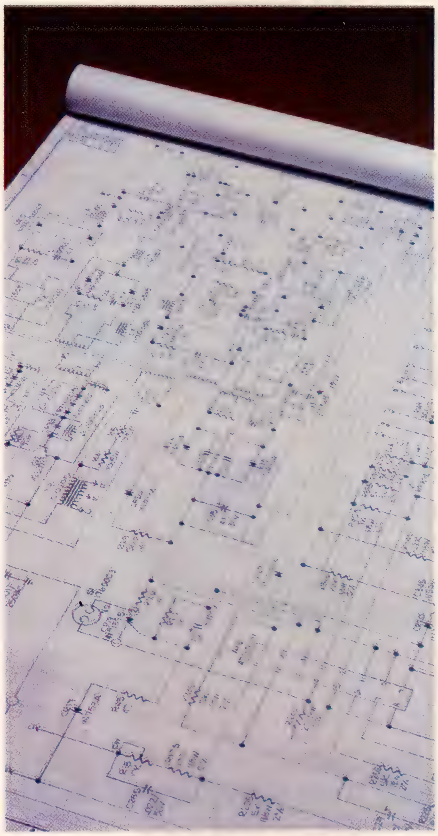

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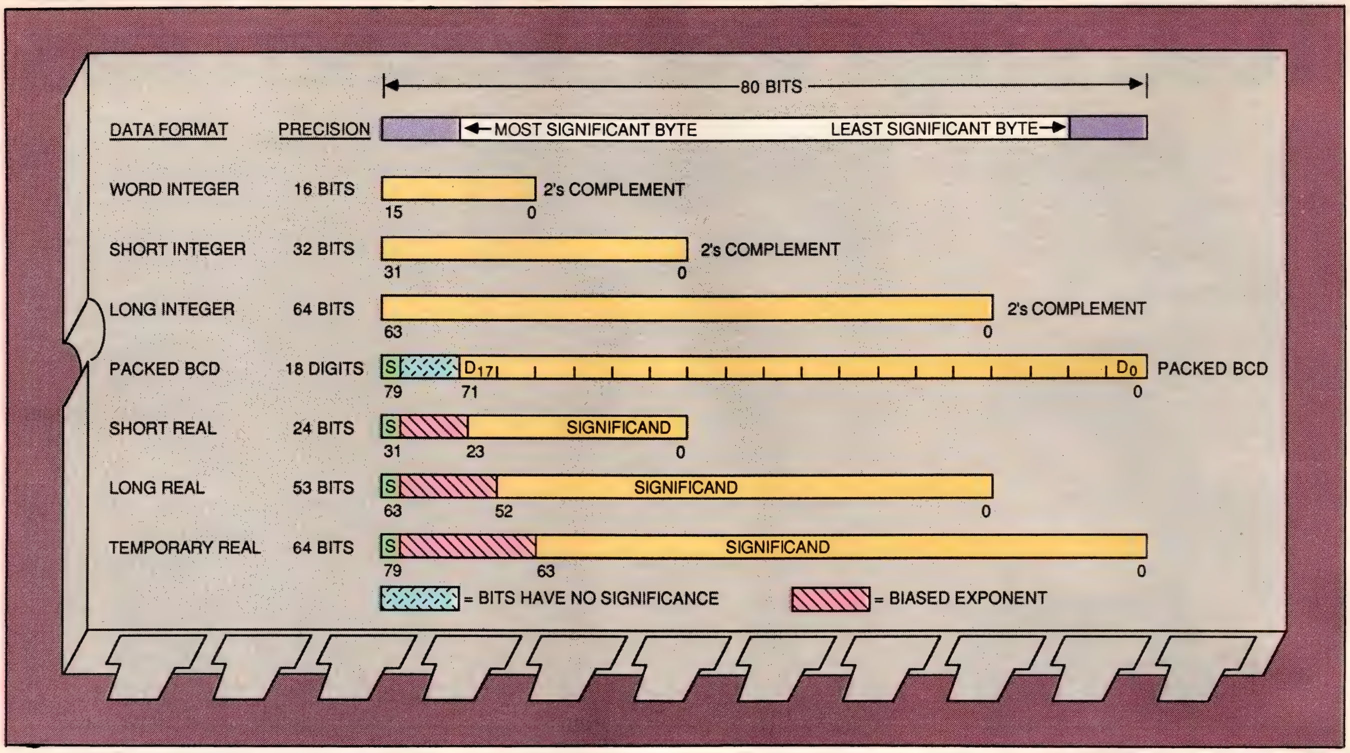

Fig 1—Data formats for FPC chips let you save values *in integer, binary-coded decimal (BCD), or floating-point (real) formats. You can choose the precision you need for each operation. Most FPC chips automatically reformat data and let you mix data types in math operations.*

(Fig 1). Except for National's NS32081, all FPC chips furnish 80-bit registers that store temporary-real values. At first glance, the NS32081's 32-bit registers seem to limit the values the chip can handle. However, instructions let you configure register pairs into 64-bit storage locations that can contain double-precision floating-point values. In almost all applications, 64-bit registers provide sufficient data-handling capabilities.

Whether a math chip furnishes internal 80- or 64-bit registers, the range of values you can store in each type of register is extremely large. For example, the 80-bit temporary-real storage registers can contain values that range from numbers as small as $\pm 8\times10^{-4933}$ to numbers as large as $\pm 6\times10^{4931}$. The shorter 64-bit double-precision floating-point values range from $\pm 2.23\times10^{-308}$ to numbers as large as $\pm 1.8\times10^{308}$. As a comparison, consider the range of values available in an IBM 370 computer: approximately $\pm 0.54\times10^{-78}$ to $\pm 0.72\times10^{76}$.

Although the FPC chips manipulate a large range of values, keep in mind that the coprocessor chips still represent floating-point values as binary numbers. Consequently, there are as many representable numbers between 2^1 and 2^2 as there are between 2^{15} and 2^{16}. However, the chips still provide sufficient values to represent integers exactly in the range $\pm 2^{64}$ (which approximately equals $\pm 2\times10^{19}$).

Chips translate data formats

Because the FPC chips accept a variety of data formats, you needn't translate values from one format to another before a chip processes them. As far as your software is concerned, then, integers can remain in integer format, floating-point numbers can remain in floating-point format, and so on. How the chips store their internal information is immaterial. For example, the 80287 chip always stores internal data in the 80-bit temporary-real format. The chip automatically converts the values you send it into the temporary-real format before processing them. Unlike the other chips, though, when the 80287 produces data, it translates the value into the format you request.

FPC chips also let you mix data formats or quickly convert from one format to another. The MC68881, for example, automatically reformats information as necessary so you can process values that exist in different formats. In a FADD.W #5,FP3 operation, the MC68881 chip converts the integer value (5) to a floating-point value before adding it to the floating-point value in register 3. Being able to work directly with integers is an advantage; integers require less memory than floating-point values, and they're convenient to work with.

The math coprocessor chips conform to the IEEE Task P754 data formats and operations, but internal register formats and control codes, as well as data-transfer protocols, differ greatly—with one exception. Besides operating as a math coprocessor for V-40 and V-50 µP families, NEC's CMOS µPD72191 FPC chip also operates as a replacement for Intel's earliest FPC chip, the 8087.

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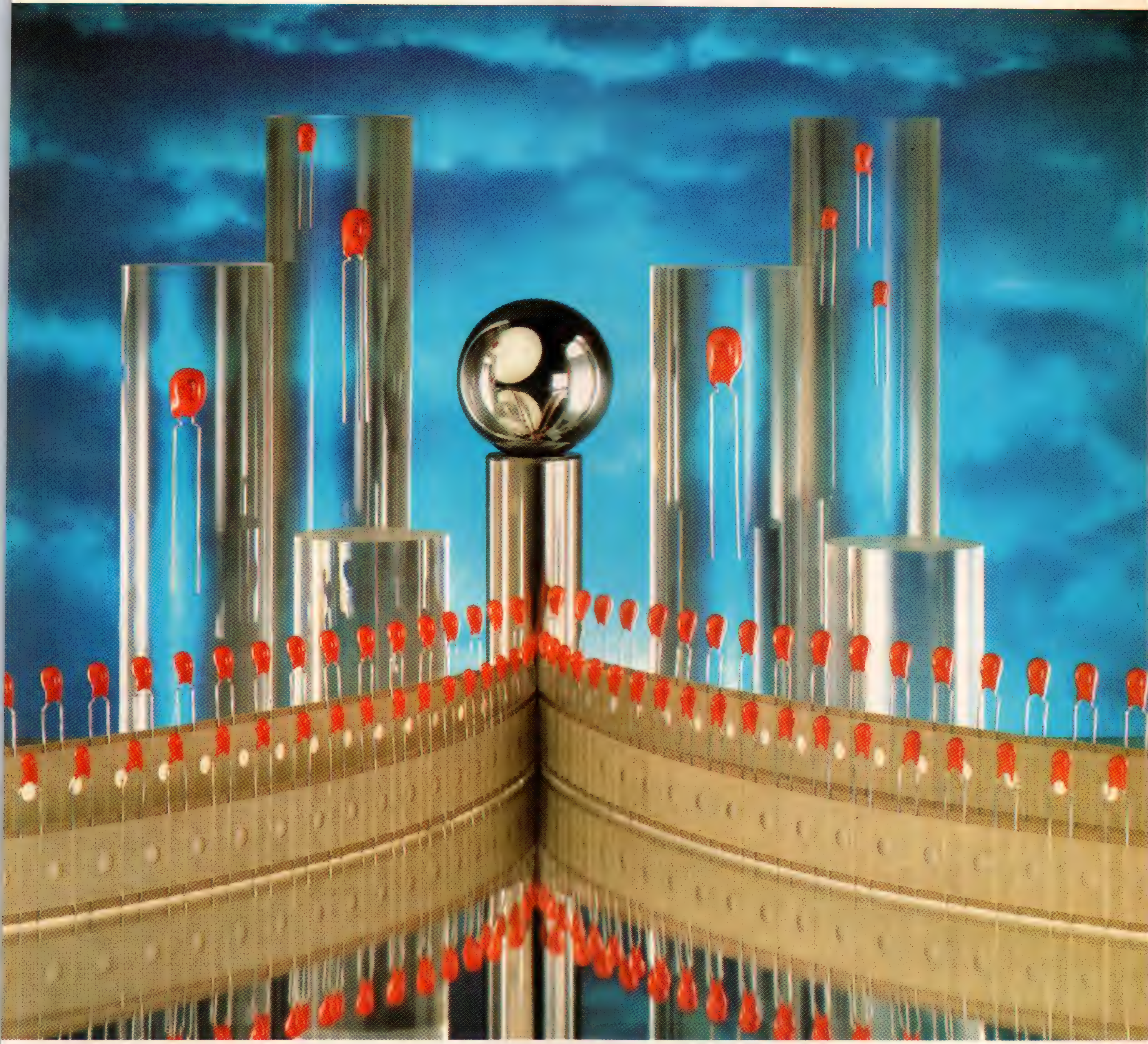

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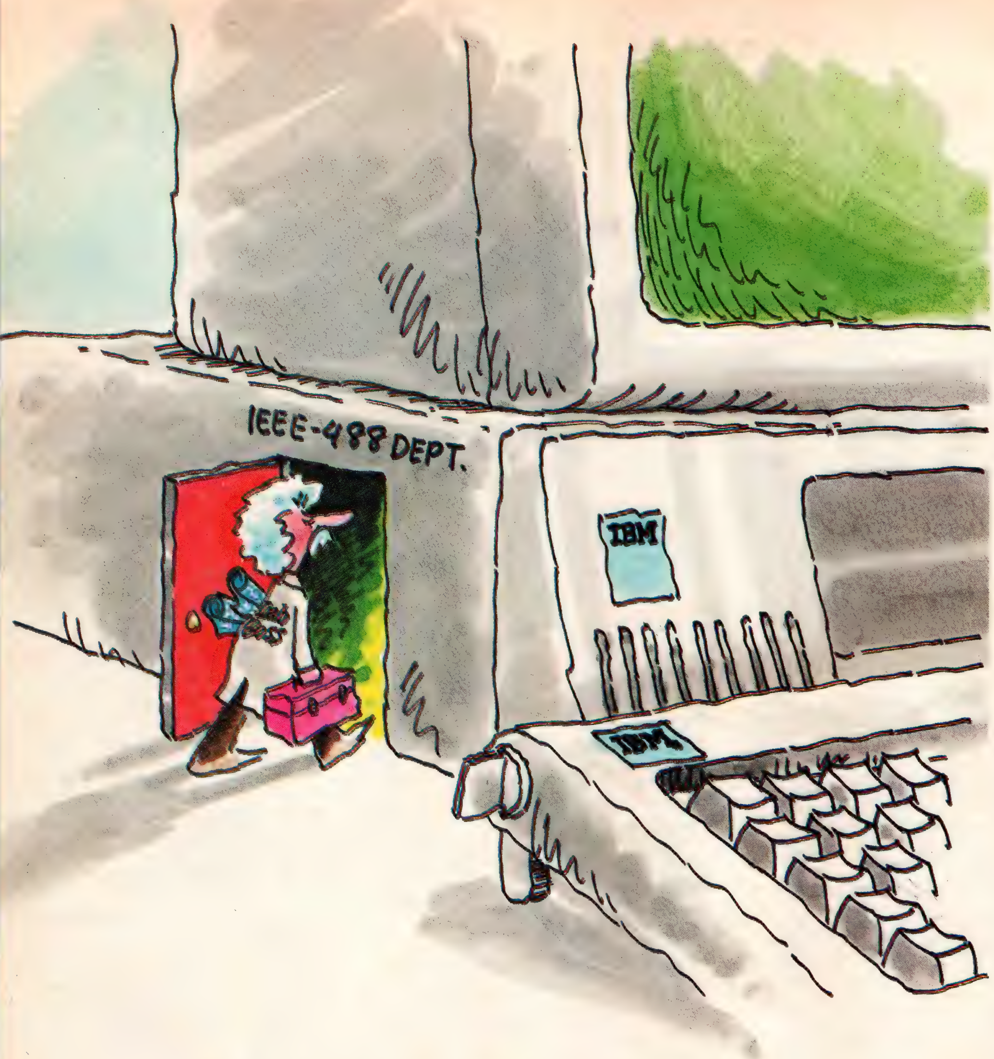

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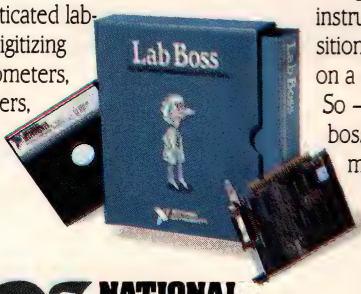

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UPDATE

NEC expects to offer sample quantities of the μPD72191 chip in the third quarter of 1986. Besides operating at a low power level, the chip will furnish additional exponential, trigonometric, and logarithmic operations that supplement those available in an 8087 chip. Logic in the NEC chip lets you select one of several operating modes that simplify interface circuit requirements.

Peripheral mode

The interface-control signals for data, control, and timing on the FPC chips let you operate them as peripherals. If necessary, then, you can adapt the chips to special computer or data-processing circuits, or you can use them in systems based on μPs that have no related coprocessor chip. However, when you operate the chips as peripherals in general-purpose μC systems or special-purpose digital systems, don't expect them to deliver top-notch performance. The host computer requires extra time to process additional memory or I/O instructions that let the required external logic circuits simulate the coprocessor control signals. The FPC chip still processes data quickly, but the extra time used for overhead-processing tasks slows the instruction- and data-transfer operations.

Bus-width incompatibilities also degrade an FPC chip's performance. A WE32106 chip requires a 32-bit data bus, so connecting it to an 8- or 16-bit computer requires additional bus buffers and data-transfer cycles that accommodate the different size buses. Motorola's MC68881 supplies two input signals that let you configure the chip's data bus for 8-, 16-, or 32-bit data buses.

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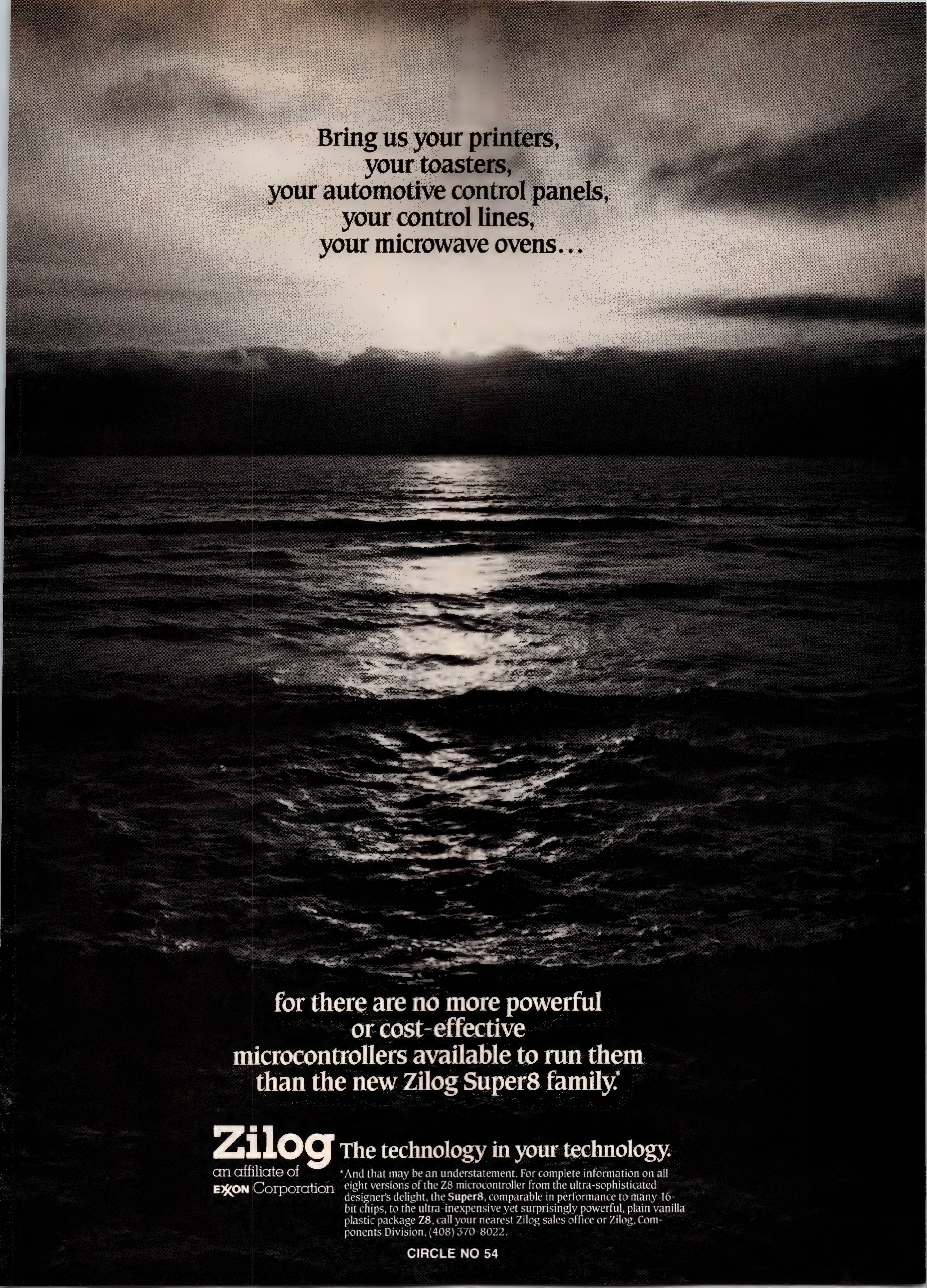

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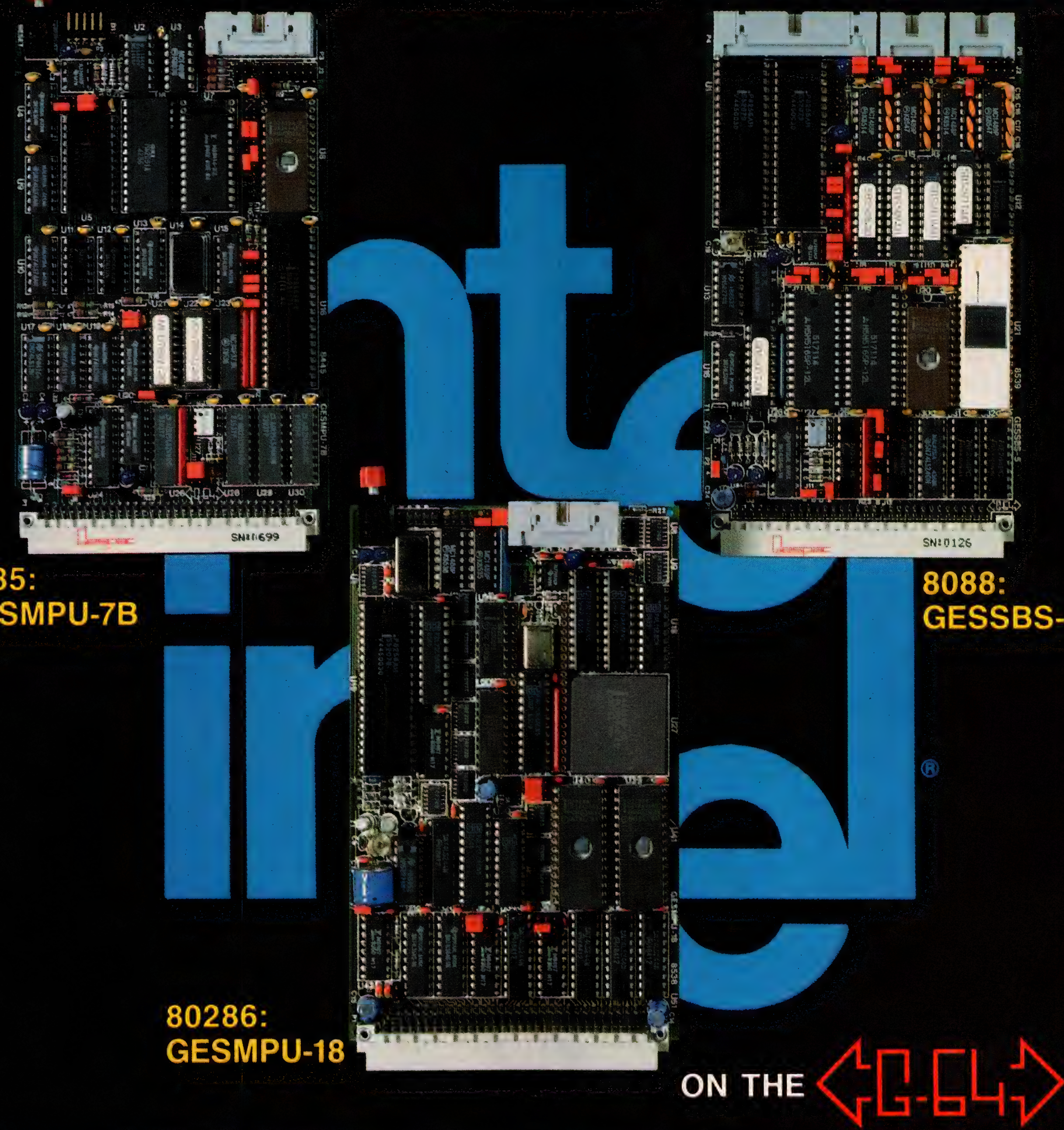

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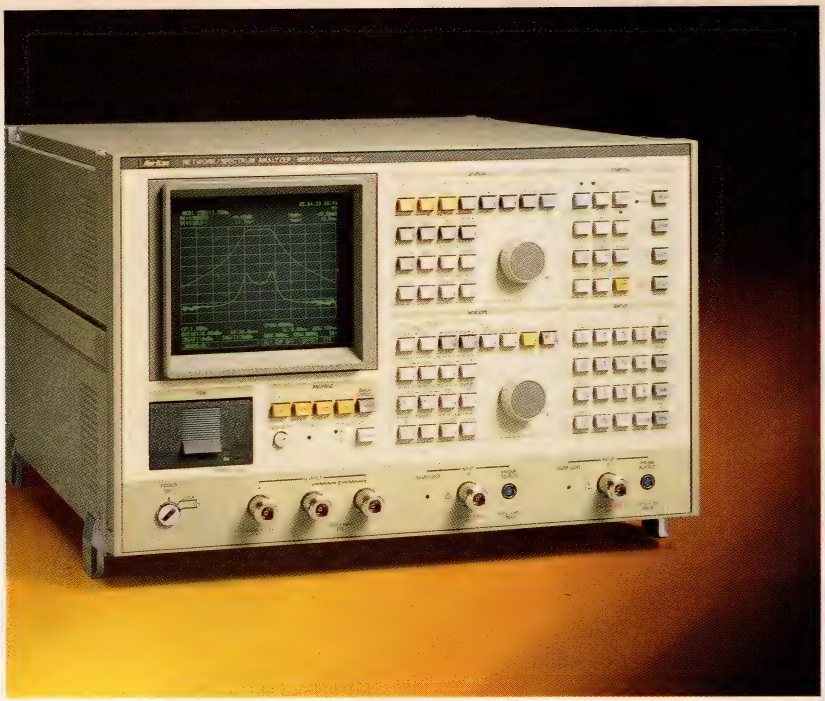

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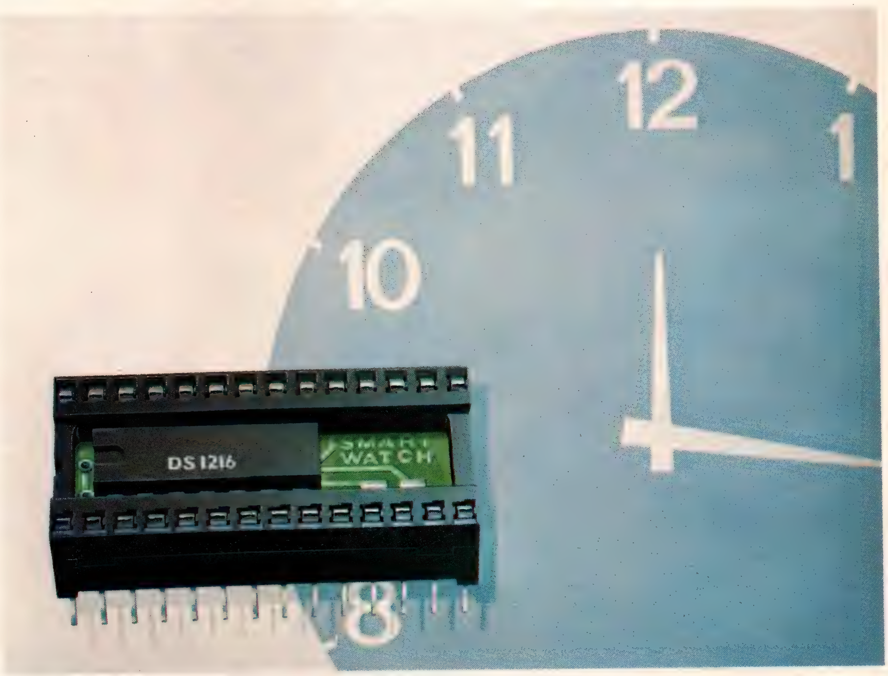
Clock/calendar chips add system features; hybrid versions vie for memory sockets

Steven H Leibson,
Regional Editor



Encased in a 24-pin socket, *the DS1216 from Dallas Semiconductor incorporates a clock/calendar and lithium battery, and it can turn a 2k- or 8k-byte static CMOS RAM into a nonvolatile memory.*

Clock/calendar IC designs now offer you features well beyond the simple ability to keep track of the date and time. Clock/calendar IC vendors have realized that the management of time is becoming more important in many microprocessor-based systems, so new chips are incorporating battery-backed RAM, watchdog timers, alarm interrupts, and power-supply monitoring and control circuitry. In addition, several manufacturers of hybrid clock modules are targeting their products at existing static RAM, ROM, and EPROM sockets, allowing you to make hardware upgrades by simply plugging in a part and revising the software.

Reading the time and date from a clock/calendar IC is not as easy as it might seem. The counters in a clock chip are usually CMOS asynchronous ripple counters, some with as many as 51 bits. Ripple time through such a long, slow counter chain is appreciable, taking several hundred microseconds. If your microprocessor happens to be extracting the time during the counter's update cycle, it could misread the data. For example, if the time is 23:59:59 and a μP reads the 10-minute digit just as the counter is clocked to 00:00:00, you may find the time misread as 23:50:00—a substantial error. This problem is called a rollover error, and it's a common problem, for you and for the manufacturer.

You can easily solve the rollover-error problem with no support from the clock chip by reading the time twice and comparing the two readings. If both readings are identical, no rollover error has occurred. However, time and date strings are often many bytes long. Reading them twice and sometimes three times (if a rollover error occurs) may take your software longer than you can allow, especially for clock ICs with slow access times, so you may wish to select a clock chip offering rollover protection in hardware.

Avoiding rollover in hardware

Manufacturers now offer four hardware aids to combat rollover error: status bits, freeze circuits, hold circuits, and capture latches. In the first case, several clock/calendar chips make available a status bit or output pin that a μP can read. If the bit is set, the counter is rippling and your software should wait for a "not busy" indication. The Motorola MC146818 (also available from RCA and Hitachi) offers a register bit indicating that the counter is being updated. Oki's MSM58321 has a $\overline{\text{Busy}}$ output pin that the chip asserts for 427 μsec while the counter is changing. Epson, SaRonix, and Statek offer the 58321 as the RTC 58321, which is integrated with a crystal in a hybrid, 16-pin DIP. Prices for these parts range from $4.89 to $8 (100).

A freeze circuit stops pulses to the clock chip's counter for a fixed period, giving the μP time to read the clock's registers before the counter is allowed to advance. By writing to register 1 of RCA's CDP1879, you freeze its counter for 250 msec, giving your software ample margin to read the date and time. If a counter-advance pulse does occur during the freeze period, the freeze circuit stores the pulse

and then advances the counter when the period ends.

Hold circuits are similar to freeze circuits, because they stop the counter when your software issues a hold command. The difference is that your software is also responsible for removing the hold condition later. Some hold circuits are activated by setting a bit in a clock chip's register, while other devices have hold pins. Panatech's RP5C01 and RP5C15 have timer-enable bits. You clear this bit to stop the counter. If a counter-advance pulse occurs, it's stored for 1 sec. When you assert the timer-enable bit, the saved pulse advances the counter.

Some of the latest time-keeping ICs have latches that capture the time and date upon receipt of a signal from the μP. Intersil's ICM7170 latches all counter bits when the 0.01-sec register is read, and the National DP8570 has a capture-enable bit called the "freeze bit," which you can use to capture the time. By setting and then clearing the freeze bit, your software can cause the DP8570 to latch the time in a block of its internal RAM.

Because most clock chips are connected to stand-by batteries, sever-

TABLE 1—CLOCK/CALENDAR ICs

MANUFACTURER	MODEL	READ ACCESS TIME (nSEC)	WRITE PULSE WIDTH (nSEC)	CLOCK RESOLUTION	DATE FUNCTION*	PACKAGE TYPE	UNUSED ONBOARD RAM
CALMOS	CA01C50	350	100	1 SEC	Y:M:DA	24-PIN DIP	NONE
DALLAS SEMICONDUCTOR	DS1215	200	170	0.01 SEC	Y:M:DA:W	16-PIN DIP	NONE
INTERSIL	ICM7170	250	100	0.01 SEC	Y:M:DA:W	24-PIN DIP	NONE
MOTOROLA	MC146818	240	300	1 SEC	Y:M:DA:W	24-PIN DIP, LCC	50 BYTES
NATIONAL SEMICONDUCTOR	MM58167A	800	950	0.001 SEC	M:D:W	24-PIN DIP	NONE
	MM58174A	900	670	0.1 SEC	M:DA:W	16-PIN DIP	NONE
	MM58274	425	350	0.1 SEC	L:Y:M:DA:W	16-PIN DIP	NONE
	DP8570	80	100	0.01 SEC	Y:M:DA:W:DY	28-PIN DIP, 28-PIN PCC	33 BYTES
	DP8571	80	100	0.01 SEC	Y:M:DA:W:DY	24-PIN MINIATURE DIP	33 BYTES
NEC	μPD1990	2000	2000	1 SEC	M:D	14-PIN DIP	NONE
OKI	MSM5832	6000	1000	1 SEC	Y:M:D:W	18-PIN DIP	NONE
	MSM58321	6000	2000	1 SEC	Y:M:DA:W	16-PIN DIP	NONE
	MSM6242	280	250	1 SEC	Y:M:DA:W	18-PIN DIP	NONE
PANATECH	5C01	400	450	1 SEC	L:Y:M:D:W	18-PIN DIP	26×4 BITS
	5C15	120	120	1 SEC	L:Y:M:D:W	18-PIN DIP	NONE
RCA	CDP1879	375	150	1 SEC	M:D	24-PIN DIP	NONE
	CDP68HC68T1	400	400	1 SEC	Y:M:DA:W	16-PIN DIP	32 BYTES
SIGNETICS	PCF8573	8700	8700	1 MIN	M:D	16-PIN DIP, SO-16L	NONE

*Y = year, M = month, DA = day of the month with automatic leap-year adjustment, D = day of the month, W = day of the week, DY = day of the year.

TABLE 2—HYBRID CLOCK/CALENDAR MODULES

MANUFACTURER	MODEL	READ ACCESS TIME (nSEC)	WRITE PULSE WIDTH (nSEC)	CLOCK RESOLUTION	DATE FUNCTION*
DALLAS SEMICONDUCTOR	DS1216	200	170	0.01 SEC	Y:M:DA:W
	DS1216E	200	170	0.01 SEC	Y:M:DA:W
ICI ARRAY TECHNOLOGY	AT-5023	120	120	1 SEC	Y:M:DA:W
LMS	C3008RHD	200	280	1 SEC	Y:M:DA:W:N
	C3008EHD	200	280	1 SEC	Y:M:DA:W:N

Y= year, M = month, DA = day of the month with automatic leap-year adjustment, W= day of the week, N = week of the year.

al vendors have added RAM to their designs, providing you with a small amount of nonvolatile memory for storing system information, such as the configuration. If you are using a clock chip that doesn't include general-purpose RAM but does have an alarm feature, you can often disable the alarm function and use the alarm registers as nonvolatile RAM.

Alarm capabilities in clock/calendar ICs range from none at all to the quite sophisticated. Intersil's ICM7170 has an 8-register comparison RAM for the alarm time. Each register has a mask bit, so you can configure the part to ignore selected portions of the date and time for the purpose of alarm comparison. Signetics' PCF8573 has a NODA (no date) flag that you can set, causing the chip to base its alarm comparison only on hours and minutes.

INTERFACE TYPE	ALARM FUNCTION	PERIODIC INTERRUPT	MIN BATTERY V_{CC} (V)	MAX STANDBY I_{CC} (µA)	PRICE (100)
8-BIT PARALLEL	YES	YES	3	200 TYP	\$10.53
BIT SERIAL	NO	NO	2.5	10	\$6
8-BIT PARALLEL	YES	YES	2.6	20 TO 150	\$6.25
8-BIT PARALLEL	YES	YES	3	50 TO 3000	\$2.25
8-BIT PARALLEL	YES	YES	2	20	\$9.25
4-BIT PARALLEL	NO	YES	2.2	10	\$8.50
4-BIT PARALLEL	NO	YES	2.2	10	\$8.50
8-BIT PARALLEL	YES	YES	2	10	\$19.80
8-BIT PARALLEL	YES	YES	2	10	\$18.90
BIT SERIAL	NO	NO	2	50	\$3.44
4-BIT PARALLEL	NO	YES	2.2	30	\$4
4-BIT PARALLEL	NO	YES	2.2	30	\$4.80
4-BIT PARALLEL	NO	YES	2	10	\$7.70
4-BIT PARALLEL	YES	YES	2.2	15	\$3.78
4-BIT PARALLEL	YES	YES	2	15	\$3.78
8-BIT PARALLEL	YES	YES	4	150 TO 2000	\$9.05
BIT SERIAL	YES	YES	3	250 TO 4000	\$4.13
BIT SERIAL	YES	YES	1.1	10	\$2.06

PACKAGE TYPE	CRYSTAL	BATTERY	ALARM OUTPUT	PRICE (100)
28-PIN RAM SOCKET	YES	LITHIUM	NO	\$19.25
28-PIN UNIVERSAL, BYTE-WIDE SOCKET	YES	LITHIUM	NO	\$19.25
24-PIN DIP	YES	NiCd	NO	\$21
24-PIN DIP (RAM)	YES	LITHIUM	YES	\$44.20
24-PIN DIP (ROM)	YES	LITHIUM	YES	\$44.20

Most clock ICs are connected to standby batteries so that they can operate while the system in which they reside is switched off. Early devices had a single V_{CC} pin, so you were required to design circuitry that switched from the system supply to the battery during power loss. The latest clock chips have separate V_{CC} and battery-supply pins, and they switch power internally. In addition, several devices offer other power-related features to facilitate system design and operation.

National's DP8570 has separate V_{CC} and V_{BB} (battery) power pins. When an internal comparator senses that V_{CC} has dropped below V_{BB}, it switches the part's internal power over to the battery after a 30- to 60-µsec debounce period. While power is available to V_{CC}, the DP8570 monitors the battery voltage on V_{BB} and asserts a low-battery status bit in a control register if this voltage falls below 2.2 to 2.4V.

You can use a separate "Pfail" input on the DP8570 to monitor V_{CC} or another power supply. When power is lost, the part generates a power-failure interrupt (if you have enabled this feature) by asserting its interrupt output pin, and it disables its bus interface to prevent loss-of-power glitches from disrupting the DP8570's registers. You can delay this disabling of the bus interface by asserting a delay-enable bit in the DP8570's routing register. Doing so gives your µP 480 µsec after the power-failure interrupt to save information in the clock's onboard RAM. If the freeze bit is asserted, the part will also save the time recorded when the power loss occurred.

Clock makes RAMs nonvolatile

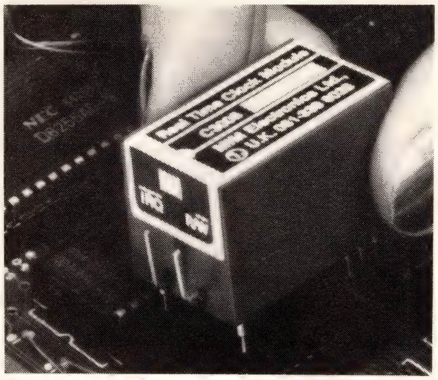
Dallas Semiconductor's DS1215 has two battery-supply pins in addition to V_{CC} for dual, redundant battery backup. When power to the V_{CC} input pin (V_{CCI}) is lost, the DS1215

switches over to the battery that's supplying the highest voltage. For single-battery designs, you connect the battery to one of the battery-supply pins and connect the other battery pin to ground.

You can also use the DS1215 to turn a CMOS static RAM into a nonvolatile memory. The part has a V_{CC} output pin (V_{CCO}), which provides power from either V_{CCI} or one of the batteries, whichever has the highest voltage. The DS1215 can disable the static RAM while V_{CCI} is lost if you place it in series with the RAM's chip-enable pin **(Fig 1)**.

You can design the DS1215 into your system using one location from your µP's address space. A proprietary serial interface designed to piggyback onto the control, address, and data lines allows you to closely couple the DS1215 to a static RAM, ROM, or EPROM. A ROM/$\overline{\text{RAM}}$ input pin determines whether V_{CCO} will switch to a battery when power is lost. This feature allows you to conserve battery power when using a ROM or an EPROM instead of a RAM.

Communication with the DS1215 begins when the device's chip-en-



You can plug the C3008E real-time clock module *(from LMS Electronics in the US or MIM Electronics in the UK) into an existing 24-pin EPROM socket and make flying-wire connections to its $\overline{IRQ}$ and R/$\overline{W}$ pins, which exit the case from the end.*

able-input ($\overline{\text{CEI}}$) and write-enable ($\overline{\text{WE}}$) pins are asserted, causing the part to compare the signal level on its D input with the first bit in its pattern-matching register. If the part detects a match, a pointer advances to the next bit in the pattern. If 64 consecutive write cycles match, the DS1215 activates, disabling the associated memory device by negating the chip-enable output pin ($\overline{\text{CEO}}$). The next 64 read or write cycles access the DS1215's registers, allowing you to dump or

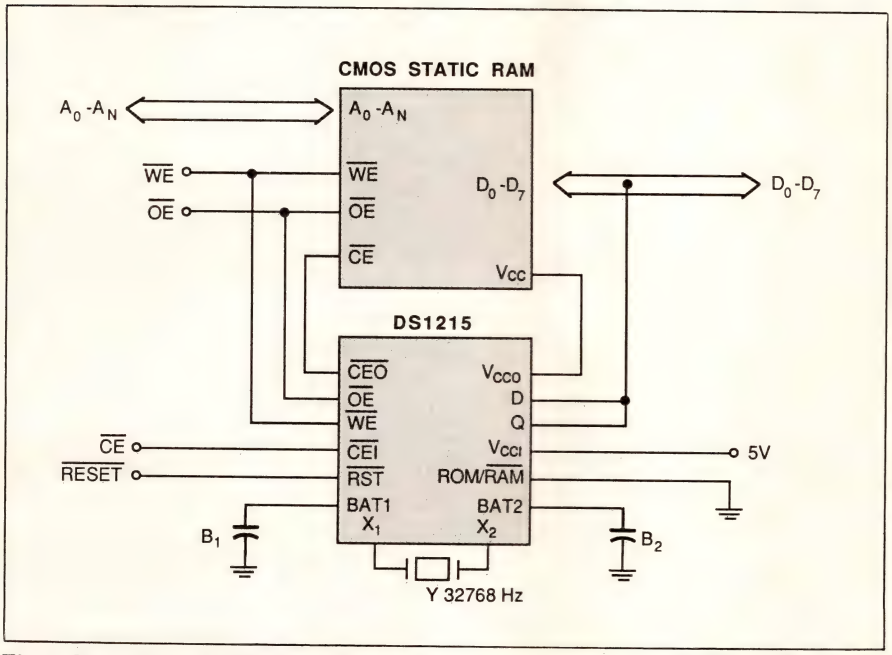


***Fig 1—You can turn a CMOS static RAM** into a nonvolatile memory by connecting the V_{CCO} pin of Dallas Semiconductor's DS1215 to the RAM's V_{CC} pin. When the DS1215 is connected in series with the RAM's $\overline{CE}$ pin, it can disable the memory whenever power to V_{CCI} fails.*

set all the registers together. You will need to allocate one address location in the memory device to handle the µP's attempts to access the DS1215.

Dallas Semiconductor offers the DS1215 in two hybrid versions: the DS1216 and DS1216E. Like many hybrid clock/calendar devices, these devices fit into memory sockets, but they offer an added attraction. Both products are 28-pin IC sockets that incorporate the DS1215 and a lithium battery. You can use the DS1216 as a socket for 2k- and 8k-byte static RAMs. When system power is lost, the RAM draws power from the DS1216's battery. Similarly, you can use the DS1216E as an EPROM socket. Because EPROMs don't have $\overline{\text{WE}}$ inputs and your data bus may not be bidirectional at the EPROM data output pins, address lines A_0 and A_2 serve as the DS1216E's data input and $\overline{\text{WE}}$ pins, respectively.

Another hybrid, the AT-5023 nonvolatile clock module from ICI Array Technology, plugs into an existing 24-pin RAM socket. An internal NiCd battery maintains the clock for three months without external power and recharges whenever V_{CC} is available. If the data bus to the socket is bidirectional, you can also use the AT-5023 in a 2732 EPROM socket, where pin 21 is the A_{11} address pin instead of $\overline{\text{WE}}$. Your software should write to the AT-5023's 12 registers at an address 2048 locations above the socket's base address, to drive A_{11} low.

LMS Electronics imports two hybrid clock modules from MIM Electronics Limited in England (Duncanfield, Cheshire). The C3008E and C3008R plug into 24-pin EPROM and RAM sockets, respectively, and incorporate lithium batteries rated for a 10-year typ operational lifetime. Both modules have an alarm interrupt output pin, which does not plug into the socket but protrudes from the end of the package. You connect this pin to your system with a flying-wire lead.

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CIRCLE NO 63

A real-time clock, three set-point timers, and an LCD allow this PCIM 2303 module from PCI to replace a μP in some designs.

The C3008E's R/$\overline{W}$ line also protrudes from the package for a flying-wire lead connection. Your data bus must be bidirectional at the ROM socket so you can write to the C3008E's data pins.

One final product is something of a curiosity in the clock/calendar IC world. If your design requires simple real-time control, you may be able to replace a μP and associated support circuitry with a $12.75 (100) PCIM 2303 timer/clock module from PCI. Housed in a plastic DIP-like case, the module has a 24-hour clock, three set-point timers with adjustable duration, and an LCD. You power the device from 1.5V; it draws 10 μA. The output signal asserts when the clock time matches one of the three timer settings or when the manual override input pin is asserted. The device will not operate with a μP, because the μP has no way to read time information from the IC. **EDN**

Article Interest Quotient
(Circle One)
High 503 Medium 504 Low 505

For more information . . .

For more information on the clock/calendar ICs and modules described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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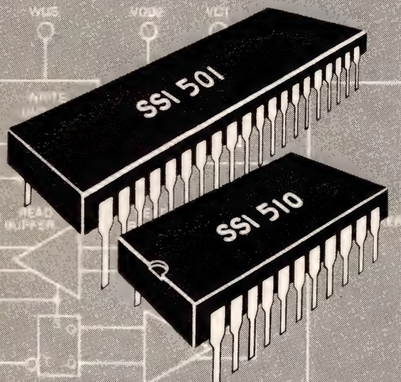

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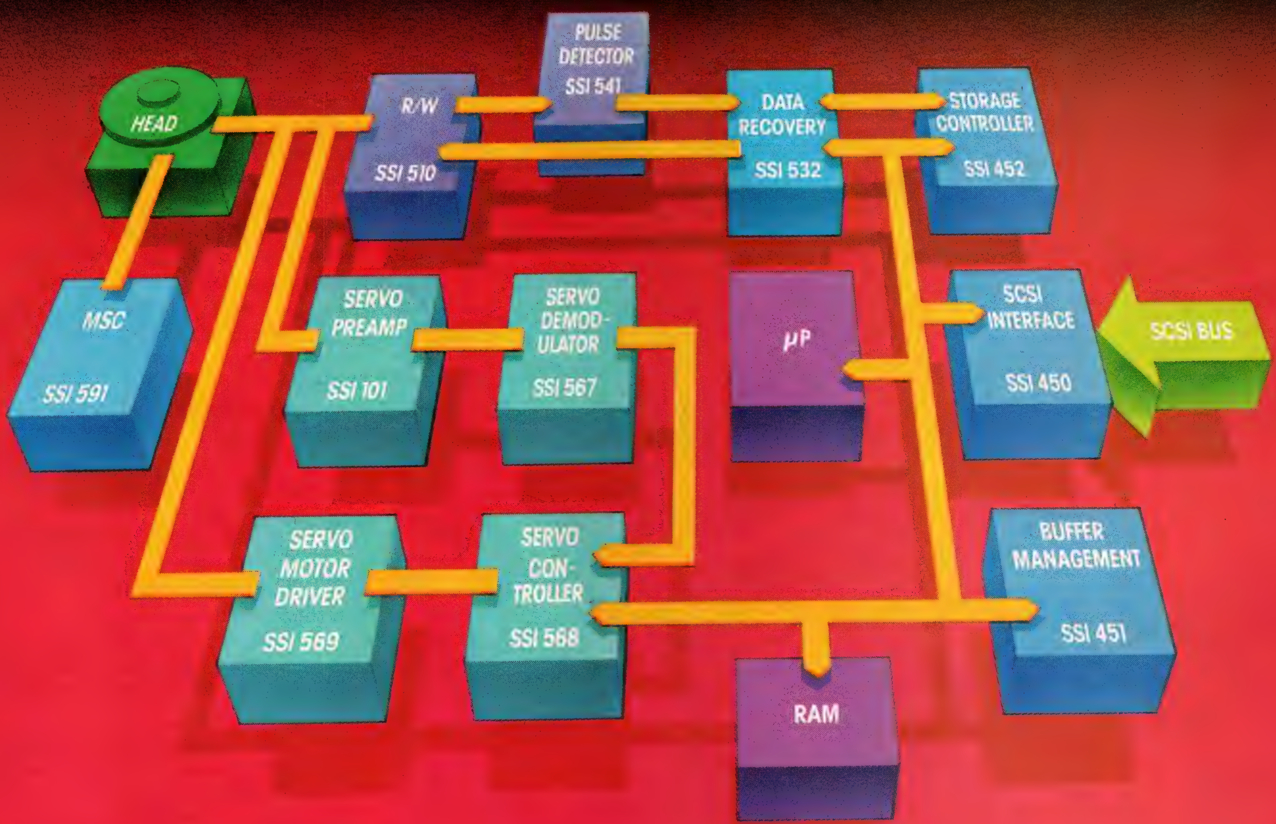

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CIRCLE NO 91

Current-output, 16-bit multiplying DAC guarantees monotonicity over temperature

A 16-bit, current-output, double-buffered D/A converter, the HS9371, offers monotonicity to 16 bits of resolution over the commercial or military temperature ranges. Moreover, the multiplying DAC consumes only 45 mW of operating power when you drive it from CMOS input levels.

A digital decoding technique using segmentation allows the HS9371 to provide monotonic operation at 16 bits of resolution. The method divides the four MSBs into 15 equal switches instead of the traditional four binary-weighted switches. The circuitry then routes the balance of 12 bits through an R-2R network. This technique reduces linearity errors arising from resistor drifts and cuts offset errors by a factor of eight.

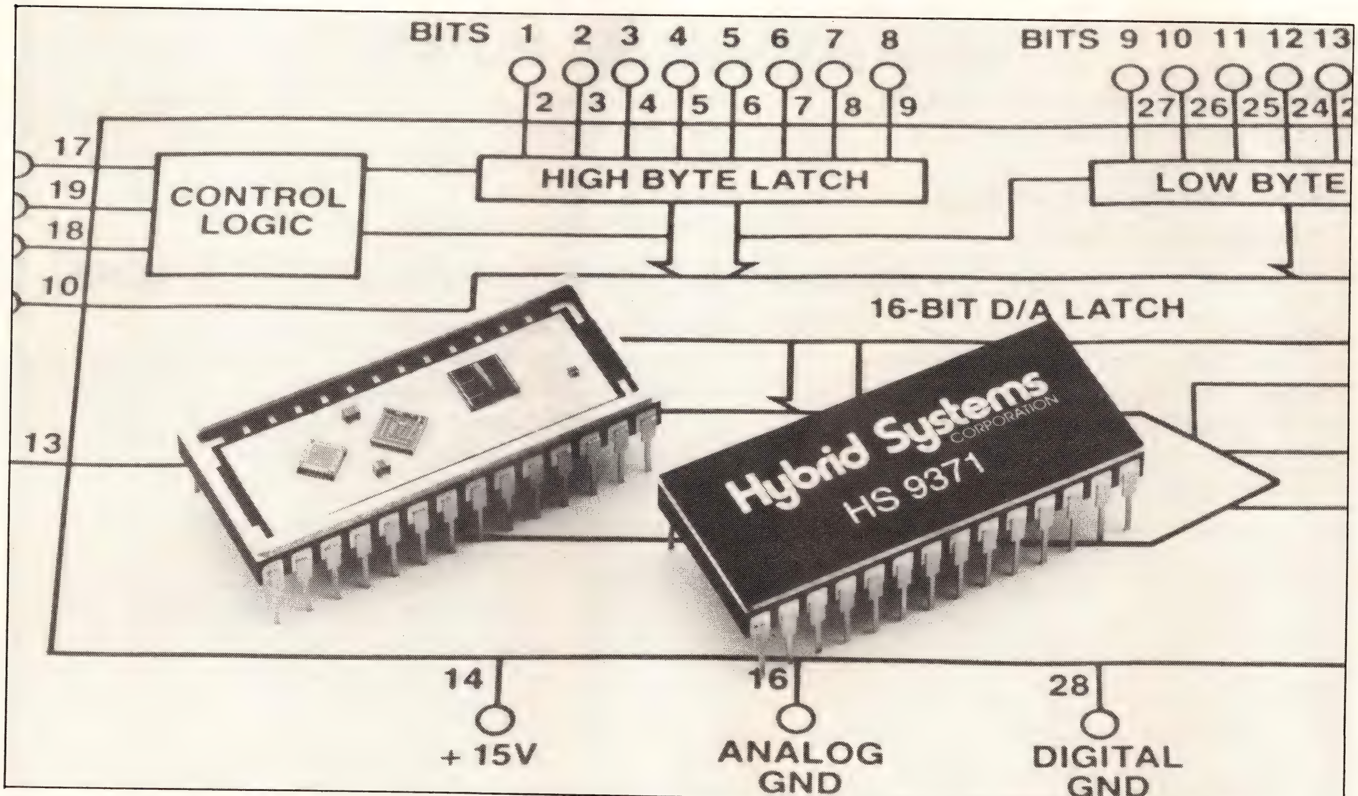
The converter's dual 8-bit input-bus structure eliminates the need for external latches. The 8-bit registers allow the device to interface to 8- or 16-bit microcomputer buses. If your system has an 8-bit bus, you can run only eight traces underneath the HS9371's package, thereby eliminating crossed bus lines and simplifying your pc-board layout.

The part's integral nonlinearity is ±0.003% max over temperature; its differential nonlinearity is ±0.0015% (1 LSB at 16 bits) max over temperature for the K and TB grades, and ±0.003% max over temperature for the J and SB grades. The converter offers 5-μsec typ full-scale-transition settling time to within a ±0.0015% error band. Its gain drift is 8 ppm/°C max, and its offset drift is 1 ppm/°C for unipolar outputs and 2 ppm/°C for bipolar outputs.

The HS9371 provides reference-feedthrough attenuation of 100 dB typ for a 100-Hz sine wave and 80 dB typ for a 1-kHz sine wave. Its glitch area is 3 nV·sec typ, and its power-supply rejection ratio is ±0.002% of full-scale range per percent of power-supply variation. The TTL-, LSTTL-, and CMOS-compatible HS9371 comes in a 28-pin double-width DIP and costs $48 to $150 (100).—***Bill Travis***

Hybrid Systems Corp, 22 Linnell Circle, Billerica, MA 01821. Phone (617) 667-8700.

Circle No 729



***Monotonic 16-bit operation over temperature** is the strong point of the HS9371 Series of multiplying D/A converters. The devices each incorporate a pair of 8-bit input latches that permit interfacing to 8- or 16-bit microcomputer buses.*

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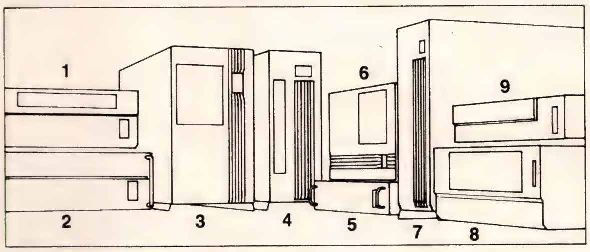

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CIRCLE NO 66

High-speed power-MOSFET driver amplifier allows you to custom tailor output stages

The Model 1464 high-speed, FET-input transconductance amplifier is designed to drive an external power-MOSFET output stage; you can thus use it to build a power amplifier tailored to your particular requirements. **Fig 1** shows a typical application circuit—an operational amplifier that provides a ±28V, ±5A output swing.

Depending on the input capacitance of the output stage that the 1464 drives, the device provides slew rates as high as 500V/μsec and a unity-gain bandwidth that exceeds 25 MHz. The 1464's high output impedance (30 MΩ typ), combined with its transconductance of 5000 μS typ, allows you to easily construct power op amps whose open-loop gains exceed 100 dB.

For the **Fig 1** circuit, the slew rate is 50V/μsec, the unity-gain bandwidth is 2 MHz, and the open-loop gain is 96 dB. Q_1 is a "V_{BE} multiplier," a configuration that imparts a temperature coefficient of approximately −3.2 mV/°C to the bias voltage for the output MOSFETs.

The pnp and npn transistors at the top and bottom of the schematic provide 6A short-circuit current limiting. You adjust R_1 to obtain the 35-mA quiescent current in the output MOSFETs; the result is a class-AB amplifier (both output devices conduct simultaneously). Alternatively, you could adjust the bias for class-B operation (both output devices are turned off in the absence of an input signal).

Input specs for the 1464 include ±5-mV max offset voltage and ±20-μV typ offset drift; the device's bias current is ±200 pA max, a figure that doubles for each 10°C temperature rise. The permissible common-mode voltage for linear operation is ±28V typ, and the common-mode rejection ratio is 90 dB min. Housed in an 8-pin TO-3 package, the 1464 operates from −55 to +125°C and costs $90 (100).

—*Bill Travis*

Teledyne Philbrick Microcircuits, 40 Allied Dr, Dedham, MA 02026. Phone (617) 329-1600.

Circle No 730

Roll your own power-MOSFET operational amplifiers *by using the Model 1464 driver amplifier. The device allows you to construct power-amplifier stages whose open-loop gains exceed 100 dB.*

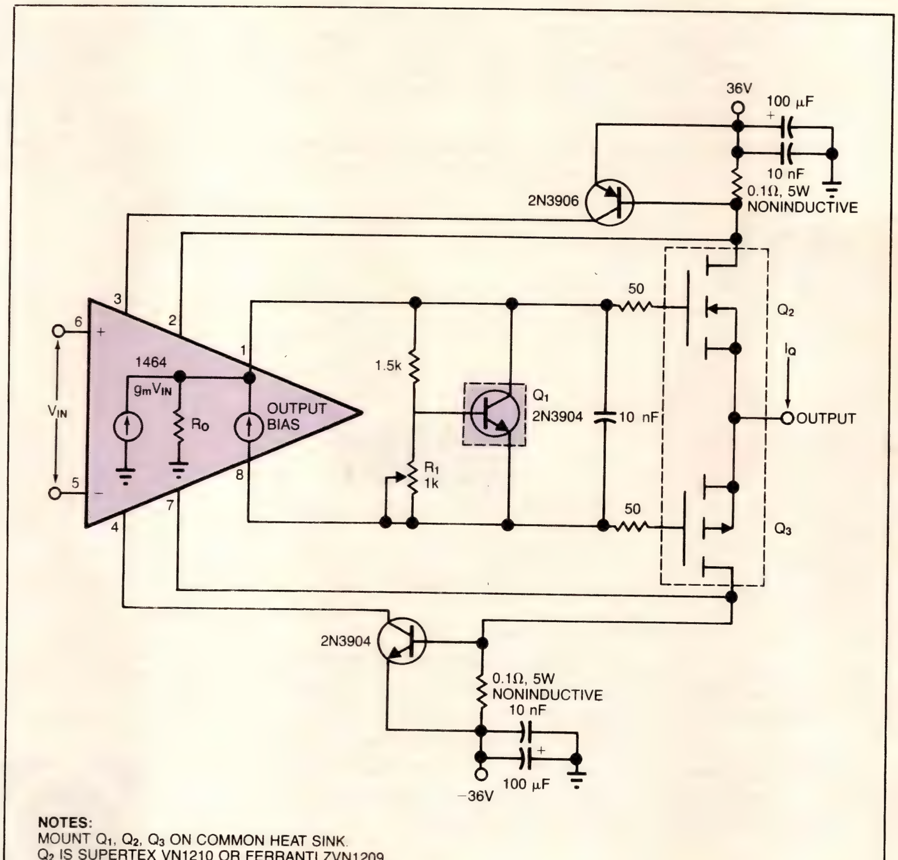
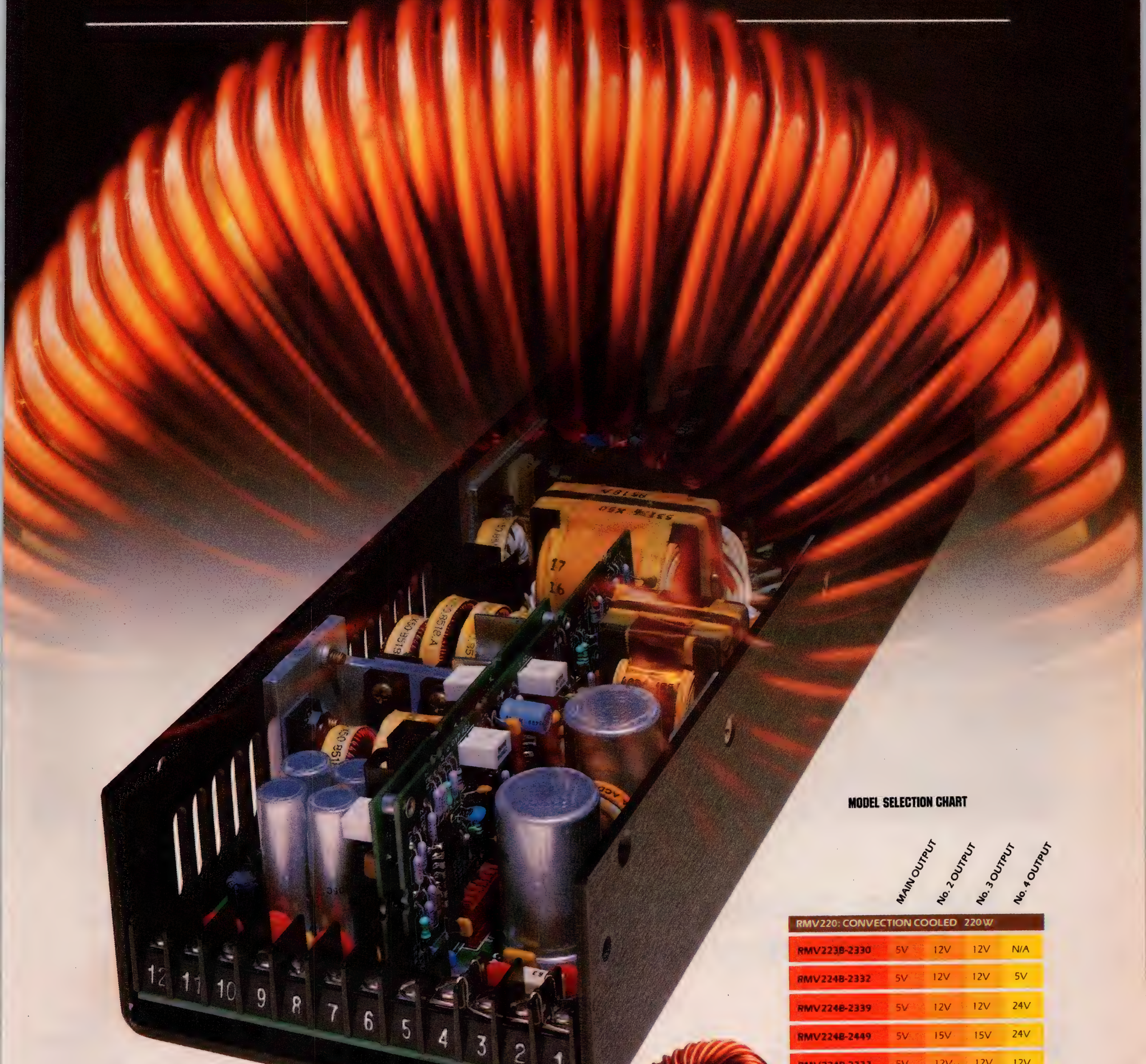


Fig 1—This typical application circuit *for the 1464 power-MOSFET driver provides 96-dB open-loop gain and delivers output swings as high as ±28V, ±5A. Q_1 provides temperature-coefficient compensation to the power MOSFETs.*

SMALL PART...BIG DIFFERENCE



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RMV224B-2332	5V	12V	12V	5V
RMV224B-2339	5V	12V	12V	24V
RMV224B-2449	5V	15V	15V	24V
RMV224B-2333	5V	12V	12V	12V

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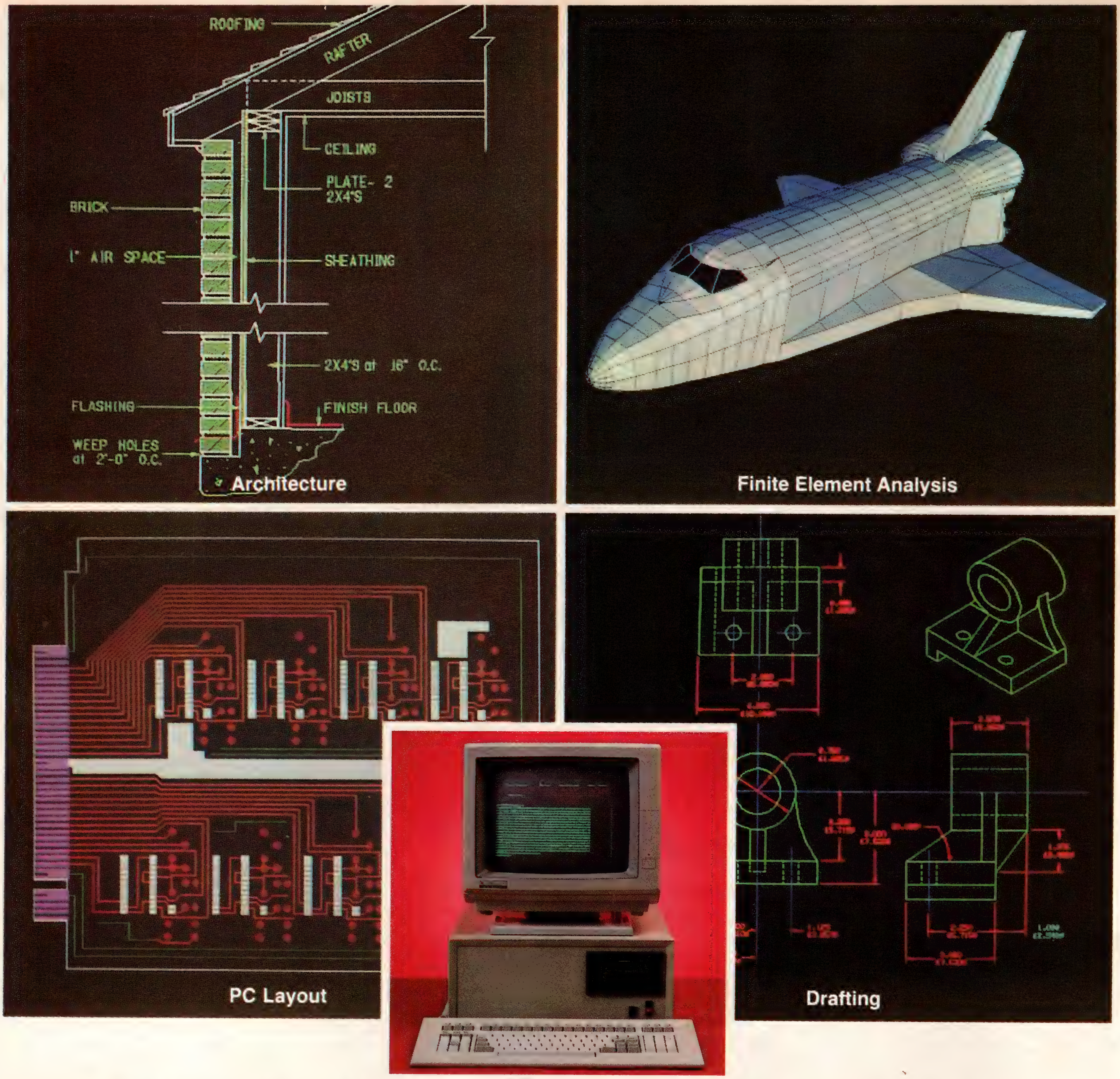

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Because it is a stand-alone workstation, you're spared from dealing with several manufacturers for different system components, as is common with most "put-together" systems. With the Lundy 2000, you're backed by a Company with a proven, solid reputation for providing fine quality graphics systems complete with service and support. The Lundy 2000 is as dependable and easy to operate as it is effective. All of this power is packaged as a highly compact turnkey system.

Application Flexibility

The Lundy 2000 workstation gives you fast, high quality design for finite element analysis, solids modeling, PC layout, mechanical design, and architectural applications, as well as business graphics and word processing. It displays up to 256 colors from a palette of 16.7 million and provides a 1536 × 1024 addressable map with 768 × 512 displayable resolution. Dual processor architecture and a high speed vector generator combine to provide full pan, zoom, and preview capabilities. This gives you operational flexibility to handle special graphics processing needs not met by standard host-dependent terminals.

For more information, contact: Graphics Marketing, Lundy Electronics & Systems, Inc., One Robert Lane, Glen Head, N.Y. 11545. (516) 671-9000.

LUNDY®

CIRCLE NO 68

Frequency-inverter IC scrambles, descrambles voiceband communications

To secure speech transmissions against eavesdroppers, you could scramble the speech information by rearranging its frequency spectrum. This technique has particular application for radio-link transmissions—for example, in land mobile radios, cellular radios, or cordless phones—in which it's relatively easy for third parties to tune in to the transmission frequency.

The FX204 variable-split-band frequency-inverter IC performs scrambling or descrambling of speech on one chip. The IC splits voiceband information into high- and low-frequency bands and then inverts each band around its center frequency. The FX204's switched-capacitor filters split the frequency spectrum, and its balanced modulators perform the frequency inversion of each band. All clocking information for the filters and modulators comes from a single external 1-MHz crystal that you can connect directly across two of the IC's pins.

Five CMOS-compatible latched programming inputs allow you to program the device's internal clock dividers to produce one of 32 different voiceband-frequency split points between 350 Hz and 2800 Hz. You can hard-wire these inputs to produce a fixed-code scrambler, or you can dynamically change them during the transmission to produce a rolling-code scrambler.

The IC's Transmit/Receive control input optimizes the internal operation of the FX204 for scrambling or descrambling. To recombine the upper and lower frequency bands and provide a low-impedance audio output, the IC has an on-chip summing amplifier with external gain-defining resistors.

The FX204 requires a transmission-channel bandwidth of 300 Hz to 3400 Hz; however, it reduces the upper bandwidth limit of the transmitted speech frequency to 2700 Hz. This reduction in effective speech-frequency bandwidth occurs because the FX204 separates the high- and low-frequency bands, internally shifting the high-frequency band by 700 Hz in order to reduce spurious outputs.

You can operate the device over narrower transmission-channel bandwidths—for example, the 3-kHz bandwidth used for mobile radio—by reducing your external crystal oscillator's clock frequency. The audio input is capable of handling a maximum input signal of at least 340 mV rms; the dynamic range is 25 dB typ.

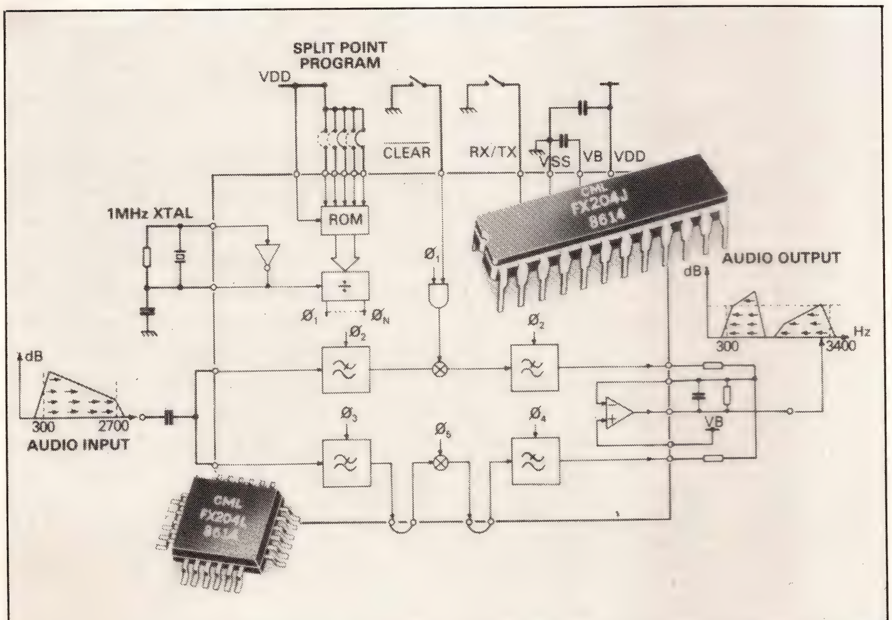
Fabricated in CMOS technology, the FX204 operates from a single 5V supply. It draws 3 mA typ (10 mA max) of supply current, so it's suitable for use in battery-powered equipment. Supplied in a 24-pin ceramic DIP or a surface-mount flat pack, the FX204 sells for between £8 and £9 (1000).—***Peter Harold***

Consumer Microcircuits Ltd, Wheaton Rd, Witham, Essex CM8 3TD, UK. Phone (0376) 513833. TLX 99382.

Circle No 731

Mx-Com Inc, 4800 Bethania Station Rd, Winston-Salem, NC 27105. Phone (919) 744-5050.

Circle No 732



Suitable for fixed- or rolling-code speech scramblers, *the FX204 frequency-inverter IC splits speech into low- and high-frequency bands and then inverts each band around its center frequency.*

Linear/digital bipolar array IC combines 6.5-GHz npn transistors and 500-MHz gates

Quickchip 4 comprises both digital circuitry and linear components; the latter includes npn transistors that achieve a gain-bandwidth product f_T that equals 6.5 GHz—the highest f_T of any array transistor. To design and simulate circuits for the arrays, you use the vendor's libraries of digital cells, digital circuit models, and analog device models.

The Quickchip 4 combines the technologies of two of the vendor's ICs: its Quickchip 2 linear array and its TECL digital array. Quickchip 4's linear components include 294 npn transistors, 174 pnp transistors, 1290 implanted resistors, and 16 programmable capacitors with values as high as 2.7 pF. In addition, the vendor can fabricate on-chip nichrome resistors that exhibit a 12% tolerance (at 25°C) and a temperature coefficient of 125 ppm/°C max. All resistor values match to within 1%; laser trimming permits tolerance and matching specs as low as 0.01%.

Design with ECL cell library

The chip's 500-MHz digital section consists of 32 ECL circuit blocks that can implement one or two of the functions in the cell library. You have a choice of SSI logic cells, multiplexers, decoders, latches, and flip-flops. Typical propagation time through the cells ranges from 400 psec for the SSI logic to 1.1 nsec for a 2-bit full adder. The ECL logic requires a −5.2V±5% power supply.

You can configure each of the eighteen digital I/O cells for either TTL or TECL signal levels. (TECL signals are compatible with 10K ECL circuits over the commercial temperature range and with 100K ECL circuits over a more restricted temperature range.) You can use the chip's analog components to implement interface circuitry for other signal levels.

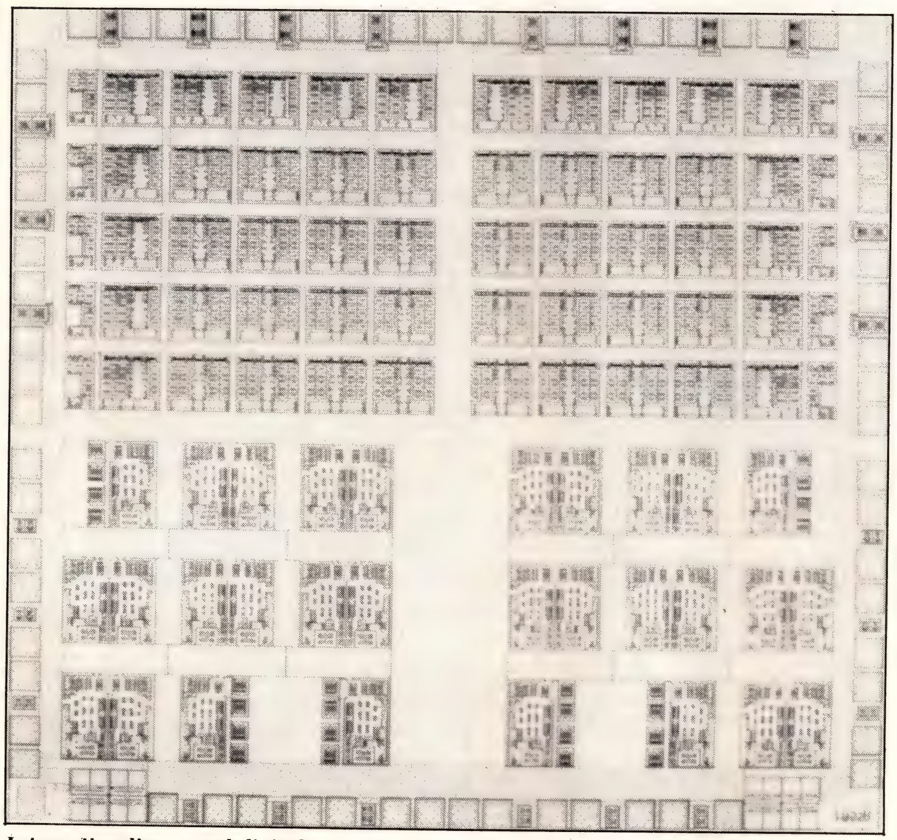
The chip contains 66 contact pads, 10 of which must connect to voltage supplies. The vendor can provide fabricated arrays as wafers or in a variety of packages, including leadless chip carriers and custom hybrids.

The company uses a design system for the chips that includes the TLogs simulator for functional, timing, and testability analysis, the TSpice circuit simulator for analog simulation, and Quickic layout software. The design system runs under the VMS or Unix operating systems.

Quickchip 4 wafers are available three weeks after you approve the final design. Packaging the parts takes an additional few days. NRE charges depend on the complexity of the design; fabrication of prototypes costs $26,500.—***David Smith***

Tektronix Inc, Integrated Circuits Operation, Box 500, Mail Station 59-420, Beaverton, OR 97077. Phone (503) 627-2515.

Circle No 733



Integrating linear and digital components *onto one IC, the Quickchip 4 includes a linear portion (top) that contains 294 npn transistors; the TECL digital portion (bottom) contains the equivalent of 300 2-input logic gates.*

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CIRCLE NO 70

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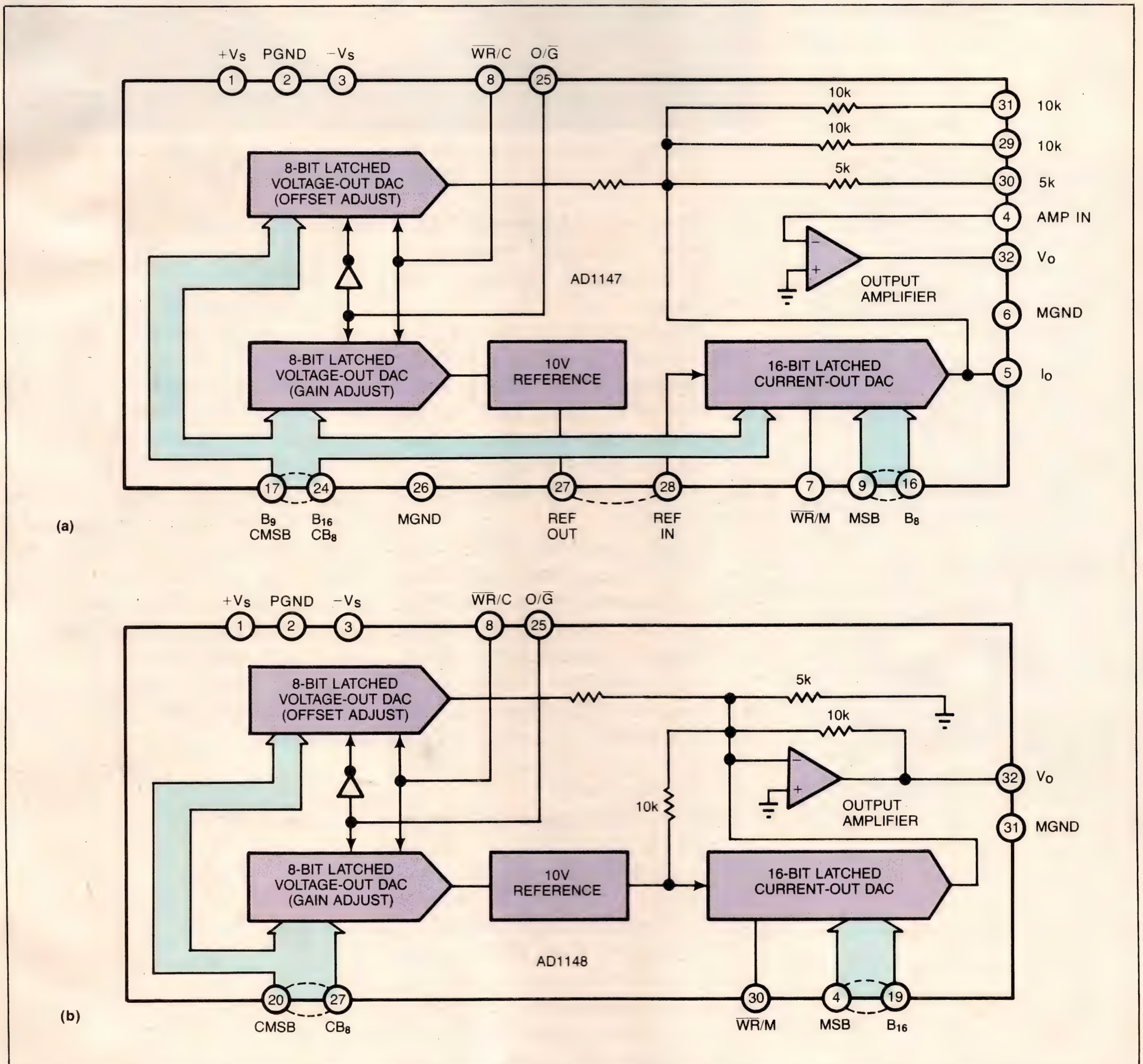
CIRCLE NO 71

Latch-input hybrid 16-bit D/A converters incorporate gain- and offset-nulling DACs

Two 16-bit D/A converters are the industry's first to incorporate internal digital-correction D/A converters to eliminate initial offset and gain errors without the need for manual trimming. The two latched-input DACs in the AD1147 and AD1148 provide the correction under the control of a microprocessor.

Model AD1147 has two 8-bit input ports. The device multiplexes both correction DACs' inputs with the main converter's eight LSBs. The multiplexing frees up package pins, and the hybrid uses these pins to



Digital-correction DACs nullify offset and gain errors *in the AD1147 and AD1148 16-bit D/A converters. The AD1147* ***(a)*** *multiplexes the inputs for the correction DACs and the main converter. The AD1148* ***(b)*** *provides a separate, 8-bit data path for the inputs to the correction DACs.*

Thick-film hybrid technology provides the medium *for the AD1147 and AD1148 16-bit D/A converters. The devices offer true 16-bit linearity and monotonicity.*

provide an external-reference input, a current output, and feedback resistors for setting the unit's full-scale range.

In contrast with the AD1147, the AD1148 has an 8-bit input port for the correction DACs' inputs and a separate 16-bit input path for the main 16-bit DAC. The AD1148 multiplexes the gain-correction DAC's inputs with those of the offset-correction DAC.

Linearity specs for both models are unequivocal and sufficiently tight to guarantee monotonicity at 16 bits. The AD1147's differential and integral nonlinearity is specified at ±0.00076% (½LSB at 16 bits) max at 25°C. The AD1148's specs for these two parameters are double those of the AD1147: ±0.0015% max at 25°C.

Note that the guaranteed monotonicity for the AD1148 is valid at 25°C only. The differential-nonlinearity drift of ±1 ppm/°C max for both devices allows approximately a ±8°C deviation from 25°C for ensured monotonicity in the AD1147, and no deviation for the AD1148.

Both models offer ±20-μV/°C max unipolar offset drift, ±6-ppm/°C max bipolar offset drift, and ±10-ppm/°C max gain drift (including the drift of the internal reference). Differential-nonlinearity stability for both devices is typically ±1 ppm/°C.

The analog-output range for the AD1147 is pin programmable for voltage ranges of 0 to 5, 0 to 10, ±5, or ±10V, and for current ranges of 0 to −2 or ±1 mA. Model AD1148 is internally configured for a ±10V output. Both devices settle (to within a ±½LSB error band) in 20 μsec typ for a full-scale voltage step and 2 μsec typ for a full-scale current step. The AD1147 and AD1148 come in 32-pin, triple-width DIPs and cost $152 and $138 (100), respectively.—***Bill Travis***

Analog Devices Inc, Box 280, Norwood, MA 02062. Phone (617) 329-4700.

Circle No 728

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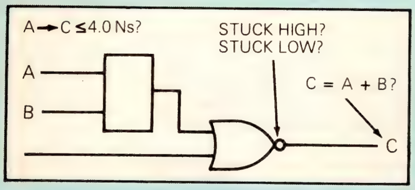

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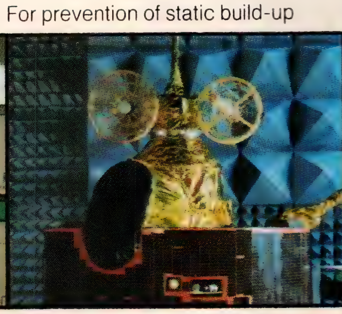

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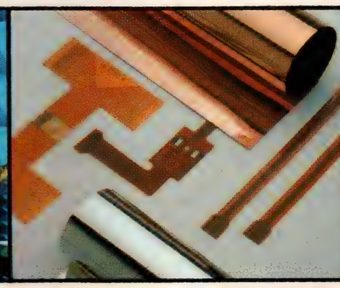

For transparent touch panels

CIRCLE NO 72

Graphics processor performs 30M flops on 1280×1024-pixel 3-D images

The Graphicon 700 manipulates 1280×1024-pixel images at rates as high as 30M flops. By implementing image-processing algorithms in hardware, the system reduces the execution time of graphics commands and of display generation. The system provides commands and primitives that you use to integrate the Graphicon into applications requiring 3-D graphics processing.

To achieve the 30M-flop processing rate, the company uses five semicustom ICs that implement geometric and image-rendering algorithms. These algorithms include perspective and orthographic projection, smooth and faceted shading, removal of hidden lines and surfaces, and illumination by multiple light sources. In addition to increasing throughput, the use of hardware algorithms reduces program complexity and memory requirements. The company claims that the Graphicon 700 can process and display a volume of cubes containing 11,664 polygons in 0.83 sec.

Serving applications requiring 3-D graphics, *the Graphicon 700 includes a desk-side graphics processor, interfaces to a host computer and peripherals, and sets of graphics primitives and commands.*

Use complex primitives

You load data describing the image (called the display list) and image-processing commands into the Graphicon 700 over an Ethernet network or one of several parallel interfaces such as DEC's DR11-W. The system comes with 4M bytes of display-list memory; you can expand that memory to 16M bytes. You describe the image using the system's 2-D and 3-D primitives, including such complex primitives as holes, cylinders, and crosshatched regions.

The system responds to 160 image-processing commands that control such system activities as display-list processing, selection of graphic-primitive and viewing attributes, display operations, and peripheral operations. Your host-resident applications initiate these commands through either Fortran or C subroutine calls.

VME Bus links processors

The system contains separate processors for I/O and peripheral control, geometric operations, and display functions. The processors communicate over the VME Bus;

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CIRCLE NO 73

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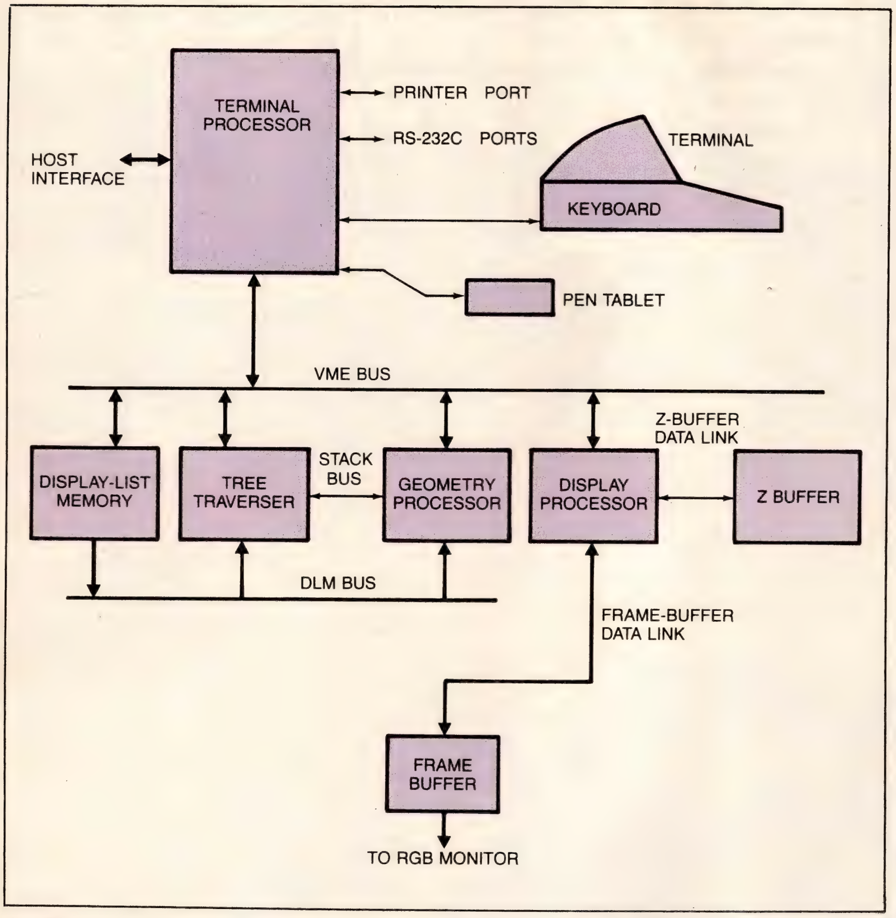
Created by Dayner/Hall, Inc., Winter Park, Florida



Multiple processors on several buses *give the Graphicon 700 a graphics-processing rate of 30M flops. The system comes with a host interface (either Ethernet or a parallel port), four RS-232C ports, a printer port, and connections to a monitor, terminal, and pen tablet.*

high-speed interaction occurs over three proprietary buses. The system includes four RS-232C ports, a printer port, and an interface to a terminal and a pen tablet.

The Graphicon 700 connects to a 1280×1024-pixel color monitor. It provides a 60-Hz, noninterlaced video image over an RGB connection. It's also compatible with 75Ω RS-343 monitors. A color look-up table allows the system to display 4096 colors out of a choice of 16 million colors.

The system comprises seven triple-wide Eurocards plugged into the VME Bus. The optional memory increases the total number of cards in the system to 10. It fits in a desk-side cabinet that measures 27 in. high, 27 in. deep, and 13.5 in. wide. The system consumes 15A max from either 115 or 230V ac power sources.

The Graphicon 700 is available 90 days ARO. The system costs $65,900, including a monitor, terminal, pen tablet, host interface, documentation, training, and support. It's also available as a stand-alone device.—***David Smith***

General Electric Company, Silicon Systems Technology Department, Box 13049, Research Triangle Park, NC 27709. Phone (919) 544-8120, x1000.

Circle No 734

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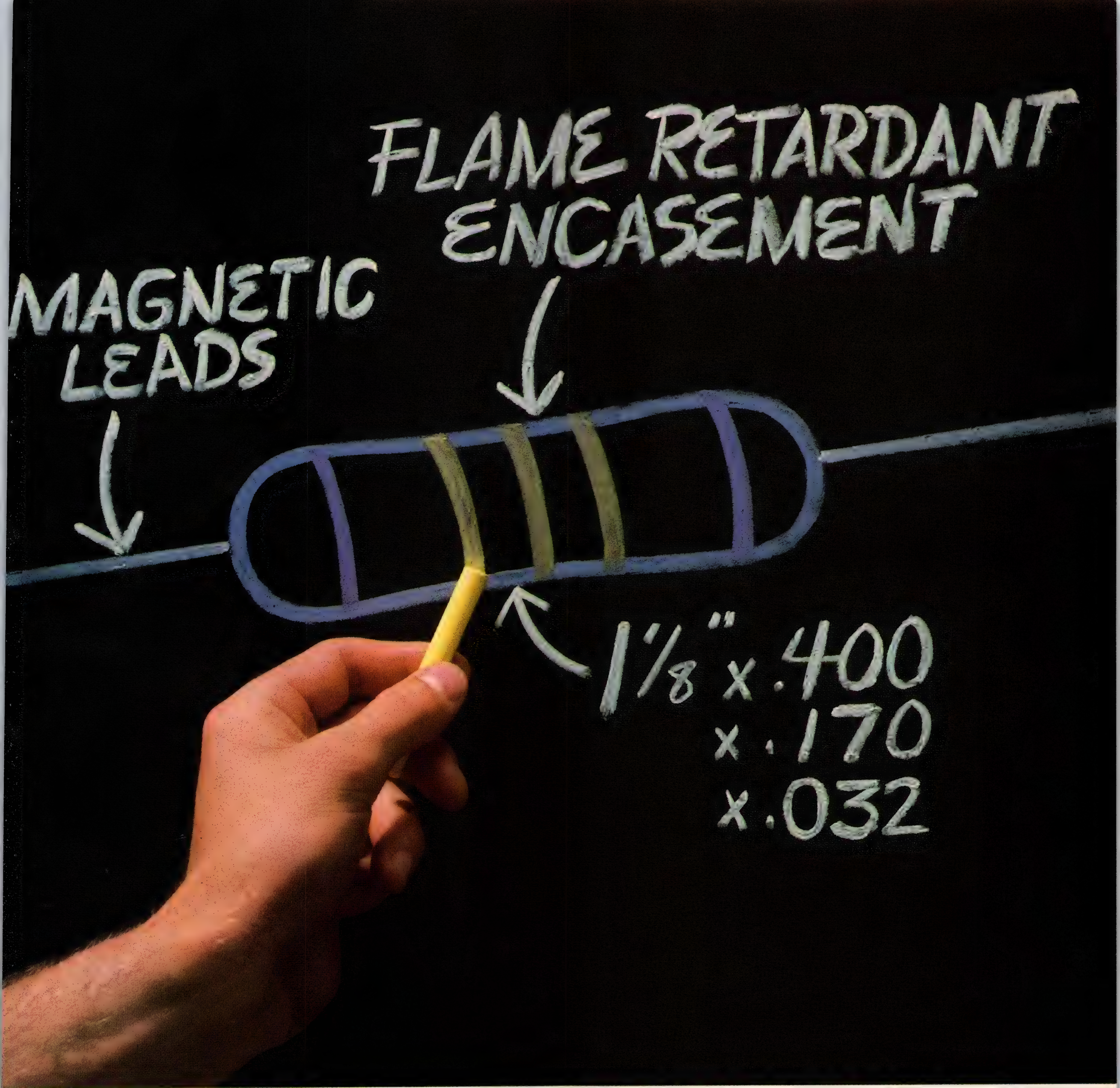
CIRCLE NO 210



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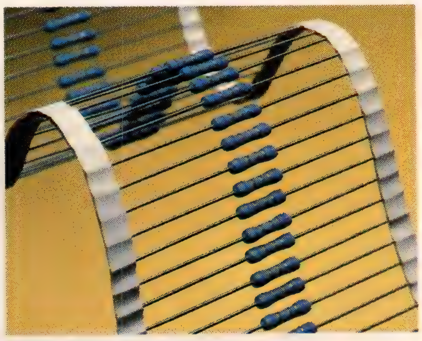

SPP Series wirewound resistors from TRW are direct drop-in replacements for low-power molded resistors. Expanded wattages available — at a cost savings of 20-25% over alternatives!

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Available in 1, 2, 3 and 5 watts down to .1 ohm with 5% to 10% tolerance, this innovative series is just another example of TRW advanced technology keeping pace with today's critical requirements.

For more information contact your local TRW distributor. Or TRW Resistive Products Division, TRW Electronic Components Group, Greenway Road, P.O. Box 1860, Boone, NC 28607. 704.264.8861.

TRW

Resistive Products Division
TRW Electronic Components Group

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CIRCLE NO 67

50-MHz memory test system handles 16M×4-bit modules

The J937 is the first integrated memory tester that can handle the latest-generation, high-speed, video and dual-port RAMs as well as 1M-bit RAMs and 16M×4-bit RAM modules. The tester operates at 50 MHz and achieves an overall system accuracy of better than 1 nsec—this resolution is an order of magnitude better than its nearest competitor's.

The tester has twelve row-address, twelve column-address, and four data lines per device. The system's pattern generator conserves test-vector memory because it can perform algorithmic operations on the test vectors in real time. The pattern generator has multiple ALUs for vector manipulation and permits sixteen levels of nested subroutines. It generates patterns for modules up to 18 bits wide.

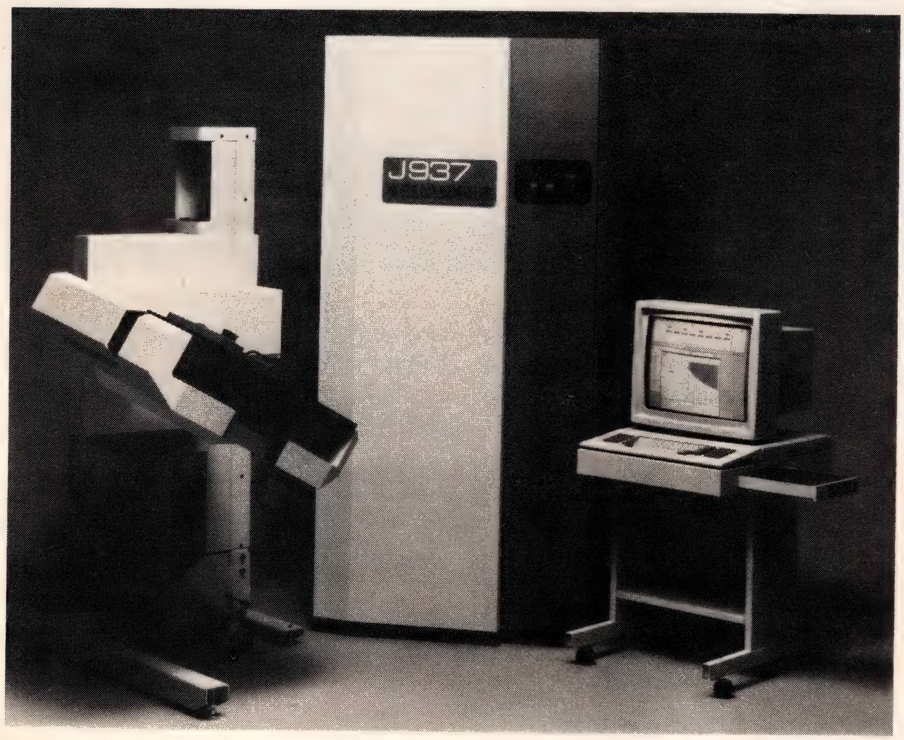
Further, the tester can retain as many as 256 independent sets of vector data and 256 independent sets of timing specifications—all selectable on the fly at full system speed. As many as 14 clocks per device-under-test allow you to test video RAMs and dual-port RAMs.

The system uses the Berkeley 4.2 Unix operating system; both operating system and testing functions are programmed in Teradyne's C-based language, T900 (a superset of Kernighan and Ritchie's C). You can interface the tester to probe stations, laser trimmers, and a host computer. Pricing starts at $360,000. Delivery, 39 weeks ARO.

—Margery S Conner

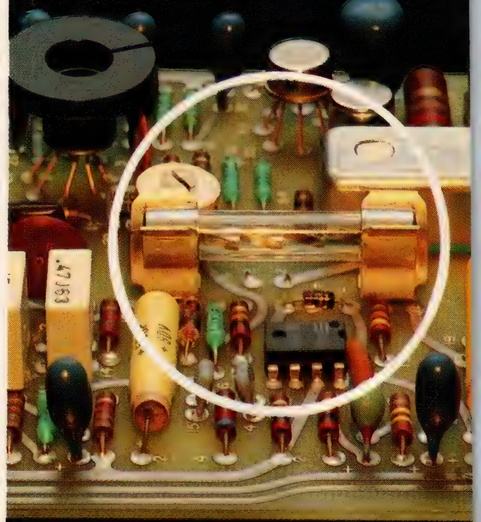
Teradyne, Semiconductor Test Div, 21255 Califa St, Woodland Hills, CA 91367. Phone (818) 888-4850.

Circle No 735

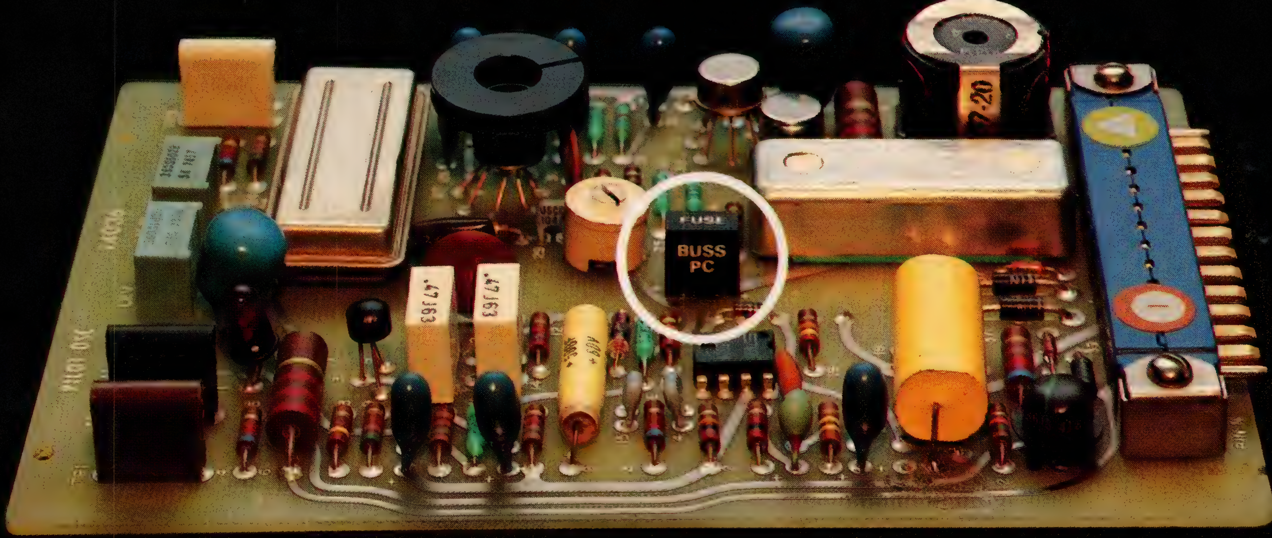


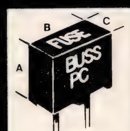
Operating at 50 MHz and having an *overall system accuracy of better than 1 nsec, the J937 tests video, dual-port, and 1M-bit RAMs at full speed.*

The fuse
you use.



The New Buss PC-Tron™ Fuse.





A = .350 in.
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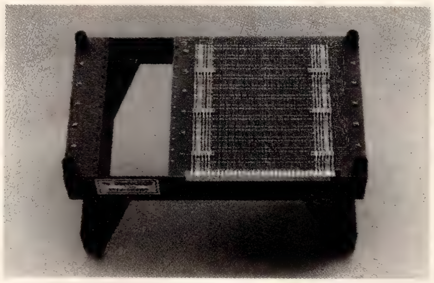
CIRCLE NO 75

100% COMPUTER TESTED MULTIBUS* BACKPLANES

Scanbe's line of U.L. recognized Micro-File™ Multibus card cages come with 100% computer-tested backplanes. And since we put them to the test before we ship—you're assured of getting great performance right out of the box. These backplanes feature provisions for mounting a –5 volt regulator and a reset switch, a parallel priority resolution (PPR) circuitry option, and an extensive groundplane.



In addition to a superior backplane, these rugged Micro-Files also feature Deep-Track (0.125") nylon card guides to assure smooth card insertion and positive connector alignment. Once the card is inserted, positive card lock-down bars keep the card secure even under the harshest conditions.

Micro-Files accommodate all standard Multibus 1 cards and are available with 3-26 card slots, plus a 4-slot pluggable expansion file. What's more, you have a choice of standard, horizontal, or vertical rack mounting. You can choose card cages with or without backplanes, with card spacing of 0.60" or 0.75," with or without fan mounting kits—all in standard or custom configurations.

For the full story on Micro-File card cages, call or send for free literature today, or order now: outside CA **(800) 227-0557**, inside CA **(818) 579-2300**.

Scanbe, Division of Zero Corporation, 3445 Fletcher Avenue, El Monte, CA 91731.

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*Multibus is a trademark of Intel Corporation.

CIRCLE NO 76

Nonvolatile memory cartridge customizes μP systems

A nonvolatile memory cartridge provides a simple way to plug custom applications into your general-purpose μP-based computer system. The DS1217M 1M-bit nonvolatile read/write memory cartridge is about the size of a credit card. The rugged cartridge suits portable applications and handling by end users.

As long as your computer system contains JEDEC 28-pin byte-wide memory sites, you can retrofit the DS1217M cartridge to your computer via a ribbon cable that's terminated with a 28-pin DIP plug. Alternatively, you can plug the DS1217M into a standard 30-pin card-edge connector that's mounted directly to the computer's pc board.

For additional storage capacity, you can stack as many as 64 cartridges on one bus. You access each cartridge in continuous 32k-byte banks. By using pattern recognition, you can switch banks from the address bus via software control.

This static-RAM cartridge can read or write 8 bits of data in 250 nsec. The DS1217M's automatic write-protection circuitry prevents data loss. A lithium battery contained in the cartridge supplies power to the RAM for as long as 10 years in the absence of an external supply voltage. For applications in which data integrity is critical, the DS1217M provides an internal isolation switch that lets you use two batteries for backup power.

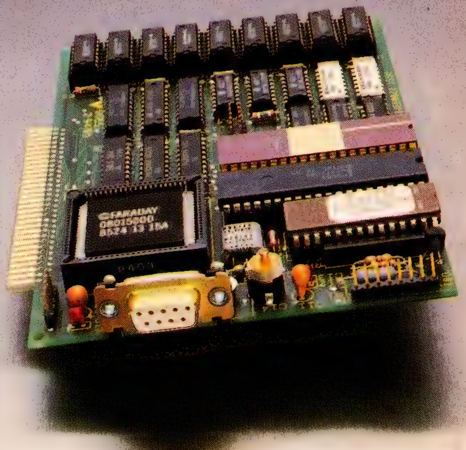
The DS1217M has a manual switch for unconditional data protection. The RAM cartridge operates over 0 to 70°C. The cartridge sells for $357.50 (100).—***J D Mosley***

Dallas Semiconductor, 4350 Beltwood Parkway, Dallas, TX 75234. Phone (214) 450-0431.

Circle No 726

You can tailor your computer system *by plugging in this the DS1217M 1M-bit, programmable, nonvolatile data cartridge. You can retrofit this cartridge to your computer for quick system integration.*

smallest



Faraday delivers the Micro PC.™ A single board computer with the capabilities of the IBM® PC but only 4.2x6.2 inches.

With the Faraday Micro PC, you can imbed the power of the IBM PC into thousands of new applications. The Micro PC features: ■ Plug-in card ■ ROM BIOS on board ■ 8088 processor with optional 8087 co-processor ■ 256K RAM memory ■ 64K ROM memory ■ CMOS version optional ■ 4.77 mhz

You can depend on Faraday to deliver 100% PC BUS compatibility. We supply OEMs in telecommunications, office automation, industrial automation, instrumentation, manufacturing test equipment, medical instruments, point of sale, computer terminals and personal computing applications.

For more information on the Micro PC or other Faraday PC BUS single board computers, call us at 408-749-1900.

Faraday Electronics, 749 North Mary Avenue, Sunnyvale, California 94086, TLX 706738. In England, TLX 847096 EMDAL.

FARADAY

Faraday quality at ⅕ the size.

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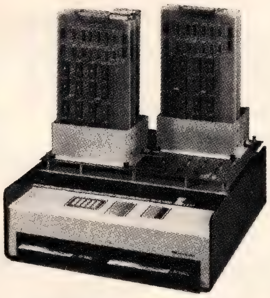
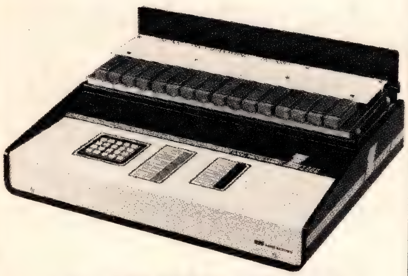
CIRCLE NO 77

AMERICA'S BEST PROGRAMMERS



Z-2500B IN-CIRCUIT MEMORY CARD PROGRAMMER

- Programs and tests up to 32 customer memory cards populated with EPROMs or microcomputers at a time.
- Two 1.2 Mbyte DSDD floppy disk drives. Optional 20 Mbyte hard disk.
- Simple menu driven operation.
- Turnkey systems include programmer, terminal, custom interface hardware and software.



Z-3000 HIGH VOLUME GANG/SET PROGRAMMER

- 14,000 27256's programmed per day.
- 32 EPROMs simultaneously with 1 to 8 DATA BLOCKS.
- 16 Intel or Motorola MCUs at a time.
- 64K to 256K bytes of DATA RAM.

Z-1200B TWELVE SOCKET GANG/SET PROGRAMMER

- 2716 – 27512, 1 to 4 DATA BLOCKS.
- 64K to 256K bytes of DATA RAM.
- Software personality. No plug-ins.

Z-1000B UNIVERSAL PROGRAMMER

- Over 600 PLDs, EPROMs, EEPROMs, bipolar PROMs and INTEl MCUs.
- Upgradeable PROM based software.
- Stand alone or PC/XT/AT operation.
- Two independent RS-232 ports.
- 64K or 256K bytes of DATA RAM.
- EXATRON handler interface is standard.

ZAP SERIES low cost programmers for EPROMs and single-chip MCUs.

Z-400 for bipolar PROMs and EPROMs.

SUNRISE ELECTRONICS, INC.
524 South Vermont Avenue
Glendora, California 91740
(818) 914-1926

CIRCLE NO 78

ESDI controller interfaces Winchesters to VME Bus

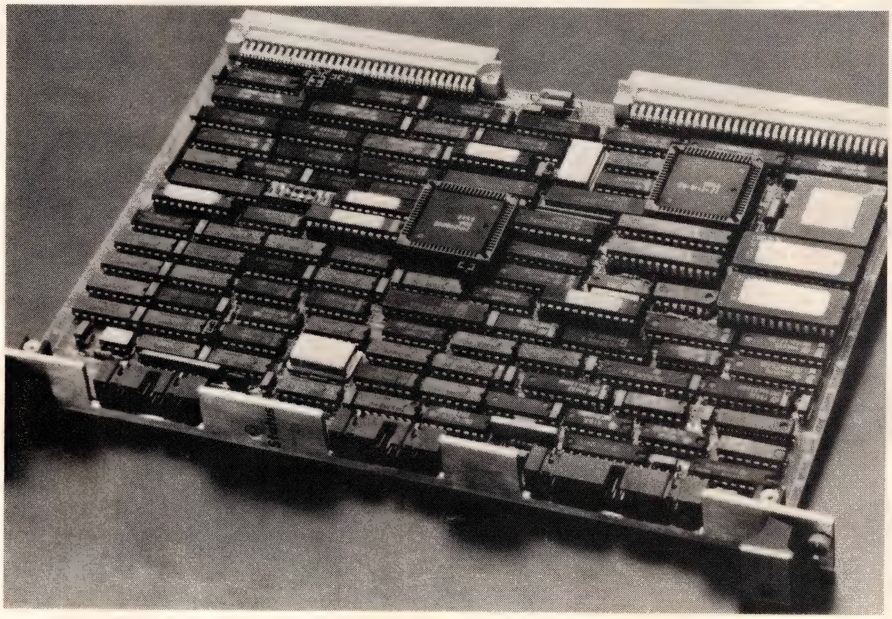
To add the performance of an Enhanced Small Device Interface (ESDI) drive to your VME Bus system, you can use the V/ESDI 3201, which offers intelligent control for 5¼-in. ESDI Winchester disk drives. The 3201, a single-board controller with a multitasking architecture, provides control for one or two drives having data rates as high as 24M bps.

The 3201 features a 68000 μP that supervises all the board's functions, including the virtual buffer activity of the controller's data-buffer pool. The board's μP-controlled virtual buffering ensures efficient buffer allocation for the various controller processes and eliminates the data overrun and underrun problems of FIFO-based controllers.

The dynamically controlled buffer pool allows the 3201 to begin reading data as soon as the drive's head lands on a data track. The board then transfers the specified data sectors immediately, regardless of the order in which it reads them. As a result, the V/ESDI 3201 never takes more than one disk revolution to transfer a track of data.

The virtual-buffer architecture provides the board's multitasking capability and reduces disk-rotation latency. The multitasking capability allows the board to perform disk and bus functions simultaneously through intelligent caching. Even after the 3201 has completed a read operation and transferred data sectors, it continues to read and cache data from the drive, reducing the number of additional disk accesses your system must make. In comparison with similar boards that use unaided 1:1 interleaving techniques, the 3201 provides greater data throughput and reduces the disk transfer time by one-third.

The V/ESDI 3201 is software compatible with the company's V/SMD 3200 controller, so you can



Providing ESDI performance for your VME Bus system, *the V/ESDI 3201 Winchester disk-drive controller from Interphase Corp also offers such features as Unix-optimized caching and virtual buffering.*

The VMEbus Story

No. 2 in a Series

Technological Leadership

Proven Technology for 16/32 Bit Applications

Independent industry analysts agree: VMEbus is the leading worldwide standard system bus with 16/32 bit capabilities. VME offers advanced technical features including:

- ☑ *Multiprocessing services,*
- ☑ *Flexible interrupt structure for real-time applications,*
- ☑ *Non-multiplexed architecture for data transfer rates of 40 mb/sec and beyond,*
- ☑ *Tough reliable Eurocard format,*
- ☑ *Asynchronous timing for high performance today, with growth and adaptability to future processors and*
- ☑ *Support of leading processor architectures (68000, 286, 32000, J-11, etc).*

VITA Leads VMEbus Growth Worldwide

With over 90 members supporting the trade association it's no wonder that VITA is leading the way for manufacturers and users in the VME Community. Each day more users select VME to guarantee success in their next system development in data communications, industrial automation, data acquisition, image processing, and many other demanding 16 and 32-bit applications.

There are currently over 200 manufacturers of VMEbus products worldwide and over 1500 different products being manufactured. These products include: microcomputer boards, subsystems, bus interfaces, software, accessories, hardware packaging, etc. VITA has recently published their Winter 1986 VMEbus Compatible Products Directory (CPD). The CPD sells for $14.95 in the US and $19.95 elsewhere. To receive your copy today, please forward payment in US dollars, drawn on a US bank to VITA at the address below.

VITA **VMEbus International Trade Association**

10229 N. Scottsdale Rd., Suite E - Scottsdale, AZ 85253 - USA
Telephone: (602) 951-8866

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Huntsville, AL **(205) 880-0444**

XYCOM, Inc.
Saline, MI **(313) 429-4971**

CIRCLE NO 79

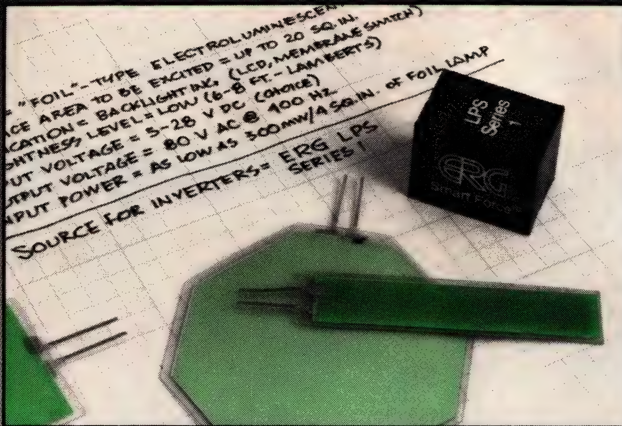
use the same drivers for either controller. The 3201 also facilitates Unix file-oriented transactions without the need for software interleaving or operating-system tuning. The controller offers 16-, 24-, or 32-bit addressing; 8-, 16-, or 32-bit data transfer; DMA with bus throttling; and 32-bit onboard error correction. You can select from seven software-programmable interrupt levels and from three bus priorities.

The manufacturer offers an evaluation reference guide that contains detailed specifications and operational data for the 3201. For hands-on evaluation of the 3201, contact the company's design-assistance group. The V/ESDI 3201 costs $1995.—***JD Mosley***

Interphase Corp, 2925 Merrell Rd, Dallas, TX 75229. Phone (214) 350-9000.

Circle No 727

SMART FORCE™ INVERTERS FOR ELECTROLUMINESCENT LAMPS... NOW, SMARTER THAN EVER



- Exclusive LPS Series 1 matrix of inverters makes foil-type EL designs easier than ever! Less expensive too.
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- LPS...from ERG — *the leader in EL power technology. More inverters for more EL applications than any other manufacturer in the world.*

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CIRCLE NO 80

IT PAYS!

Stop MIL-Spec connector damage with Glenair's Sav-Con® go-betweens.

The cost-effective protection for connectors subjected to high-wear mating-unmating cycles.

Series 94 Sav-Cons preserve the integrity of your connectors by absorbing the punishment of repeated connect-disconnect cycles during manufacture, test and checkout. Sav-Cons are the perfect solution in such applications as high-density J-boxes, telecommunications and computer packaging where bent pins can mean days of expensive rework.

Sav-Cons are available for all currently used Military and NASA circular connectors, in all shell sizes and insert arrangements covered by these specs. Mates with:

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- MIL-C-38999 Series I, II, III
- MIL-C-83723 Series I, II, III
- MIL-C-5015
- NASA 40M38277
- NASA 40M39569

To eliminate expensive, time-consuming connector repairs and maintenance, use Glenair's Sav-Cons. The money-saver. Call or write:

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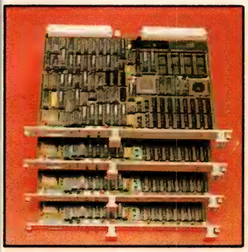
CIRCLE NO 82

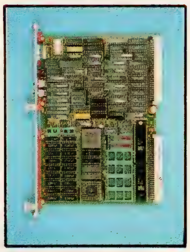
THE HI-PERFORMANCE PEOPLE — ELECTRONIC MODULAR SYSTEMS INC.

VMEbus Central Processors

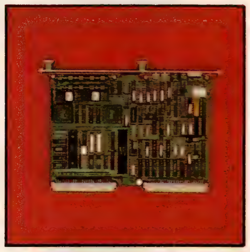
REAL TIME APPLICATIONS



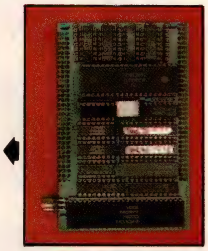
CPU-2RT



CPU-2SC



CPU-2PB

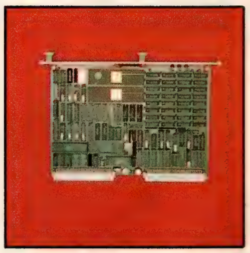


PIGGY BACK BOARDS

68020
@ 12.5 MHz,
16.5 MHz, or
20 MHz,
DRAM 1/4 Mb,
1 Mb, or 4 Mb

CPU-4RT

STAND ALONE HOST



CPU-1

CPU-3

	STAND ALONE HOST		REAL-TIME MASTER/SLAVE			
	CPU-1	CPU-3	CPU-2RT	CPU-2SC	CPU-2PB	CPU-4RT
MICROPROCESSOR	68000/68010	68010	68000/68010	68000/68010	68000/68010	68020
FREQUENCY	8MHz	12.5 MHz	12.5 MHz	12.5 MHz	12.5 MHz	12.5 - 20 MHz
MEMORY MANAGEMENT	68451	68451 (2nd as option)				
DMA	LOGIC		68450 option	68450 option	68450 option	
FLOATING POINT PROCESSOR		68881 (option)			68881 (option)	68881 (option)
RAM (DUAL PORTED)	256 Kb	2 Mb	128/512 Kb	128/512 Kb	512 Kb	1/4, 1, 4 Mb
EPROM		2 Sockets (128 Kb)	2 Sockets (128 Kb)	2 Sockets (128 Kb)	2 Sockets (128 Kb)	2 Sockets (128 Kb)
EEPROM			2 Sockets (16 Kb)	2 Sockets (16 Kb)		
SIO	1 PORT	1 PORT	2 PORTS	4 PORTS	•I/O ON PIGGYBACK BOARDS •PB-SCSI1 SCSI/DMA •PROTO BD	3 PORTS
PIO	1 PORT		1 PORT			
TIMERS	1	4/ 8 bit	3/ 16 bit			1/ 32 bit
ADDITIONAL FEATURES	1K PROM FLOPPY DISK CONTROLLER	Translation Cache	R/T CLOCK 58274	R/T CLOCK 58274		
SOFTWARE	UNIX* SYS V	UNIX* SYS V pSOS**	pSOS** PDOS***	pSOS**	pSOS**	pSOS** PDOS***

ONE YEAR WARRANTY

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**pSOS is a trademark of Software Components Group

***pDOS is a trademark of Eyring Research

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Telex: 791688 Pasadena Dal

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CIRCLE NO 83

33kHz 12-BIT DSP A/D's

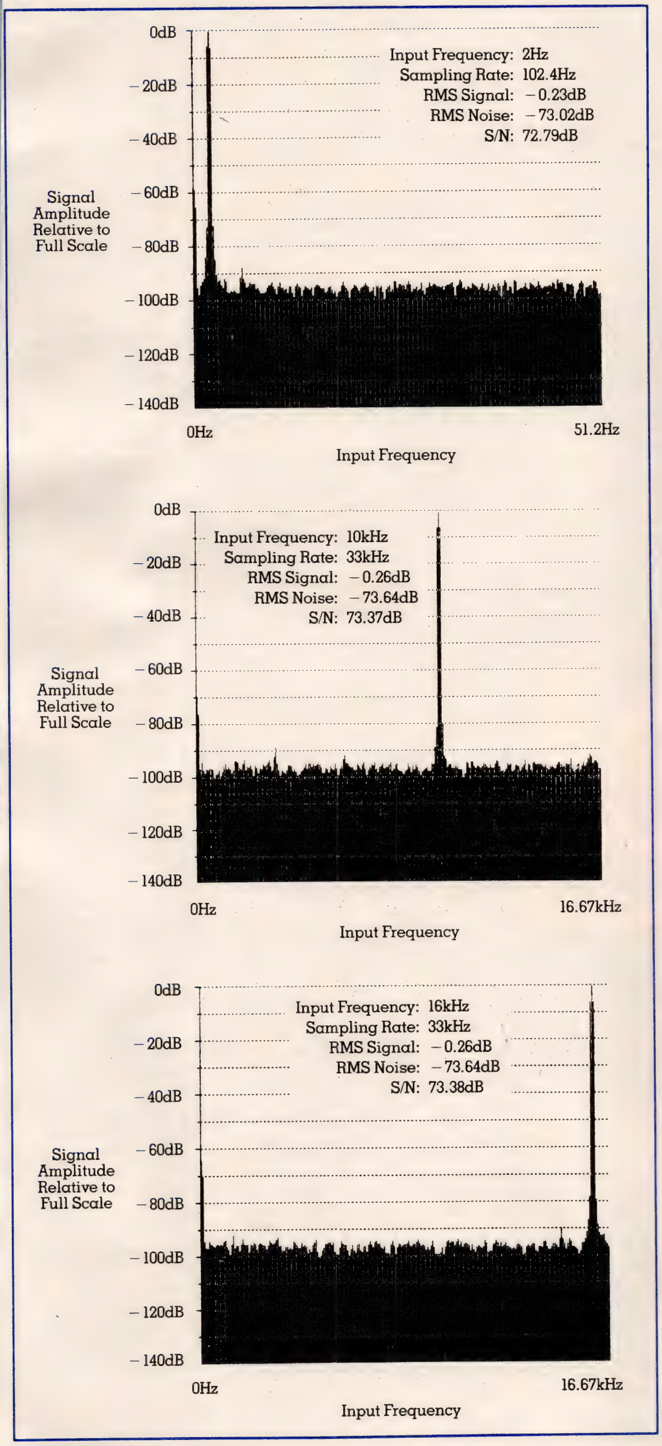
MN6227/MN6228

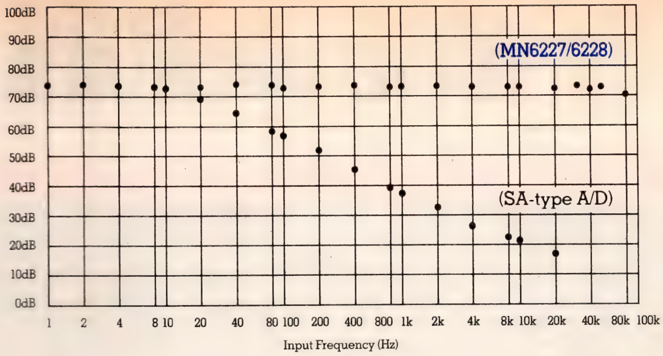
12-Bit Sampling A/D's
Sampling Rate: 33kHz Minimum
Input Bandwidth: 16.5kHz Minimum
Testing: Frequency Domain (FFT)
Signal-to-Noise Ratio: 70dB Minimum
Harmonics: –80dB Minimum
Price: $74/100's

You are looking at the *first* commercially-available, *FFT-tested*, high-speed, 12-bit, sampling A/D converters *specified* for digital-signal-processing applications. MN6227 and MN6228 are 33kHz A/D's with internal track-and-hold amplifiers. They are ideally suited for radar, sonar, spectrum and vibration analysis, voice and signature recognition, and other contemporary DSP applications. Unlike traditional successive-approximation A/D's without track-hold amplifiers, these true sampling A/D's maintain near-ideal signal-to-noise ratios independent of increasing analog input frequencies. They are *made* for the frequency domain.

Note the FFT spectra (right) and the data plot (top right). They clearly demonstrate the ability of these devices to maintain SNR with increasing input frequencies. In our frequency-domain testing, these devices operate in a manner that simulates a

digital spectrum analyzer with a known low-distortion input signal. The output spectra yield precise, practical measurements of signal level, noise level, signal-to-noise ratio, harmonic distortion, and input bandwidth… the keys to specifying for DSP applications.





This plot of actual recorded data demonstrates MN6227/6228's ability to maintain near-ideal SNR with increasing input-signal frequency, while A/D's without companion track-holds show rapid (6dB/octave) SNR degradation.

MN6227/6228 are the first A/D's in our new MN6000 series. The 12 and 16-bit converters in this series all contain internal, user-transparent, track-hold amplifiers that enable each device to accurately sample and digitize dynamically changing input signals with frequency components up to the Nyquist frequency (one-half the sampling rate).

MN6227/6228 have a full 8 or 16-bit μP interface and are packaged in small, low-profile, 28-pin ceramic DIP's, with the industry-standard MN574A pinout.

For detailed information on MN6227/6228, send for our comprehensive data sheet. For rapid response and a copy of our 384-page catalog of data conversion products, call Bob LeFort at (617) 852-5400, x297.

Micro Networks
324 Clark Street
Worcester, Massachusetts 01606
(617) 852-5400

Micro Networks
Advancing Data Conversion Technology

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A DIVISION OF **UNITRODE** CORPORATION

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The world's most advanced

CMOS macrocells have arrived.

Introducing a state-of-the-art selection of standard cells, including a 32-bit slice μP.

You can now design ASIC systems-on-a-chip using a library of CMOS LSI standard cells. Included are the world's first 16-bit and 32-bit bit-slice processor cells, EPROMs and peripherals. All manufactured using a 1.2 micron channel length CMOS process.

The LSI cells were developed by WaferScale Integration Inc. (WSI) and will be alternate sourced by RCA. WSI will also offer RCA's CMOS standard cell library.

First 32-bit bit-slice processor cell.

The 32-bit CMOS CPU cell replaces eleven discrete bipolar ICs. It beats the performance of the 2901C bit-sliced-based system by 20% and saves 97% of the power, yet it is software compatible.

The 16-bit μP slice cell runs faster than bipolar speed, and replaces five off-the-shelf bipolar devices. Without rewriting microcode. Without adding glue parts.

The 4-bit μP slice cell is functionally identical to the bipolar 2901 4-bit slice, yet runs 25% faster. You can replace the bipolar part directly for instant improvement in system performance and power consumption.

Each μP is available as a cell in the library or as a standard IC.

CMOS EPROMs.

Another new LSI cell is a 1K x 16 CMOS UV EPROM with 55ns access time. Providing on-chip microcoding capability, this cell interfaces with 8-bit, 16-bit or 32-bit buses. An intelligent algorithm allows fast programming, achieved within 4 seconds. The EPROM cell uses only 20 μA in the standby mode and only 15mA in the active mode.

And it's also available as a 70ns 8K x 8 standard EPROM in 28-pin ceramic DIP or 24-pin bipolar PROM footprint...at very competitive prices.

Complete standard cell library.

The WSI cell library has been combined with the RCA library of over 300 verified cells to give you a very broad choice of LSI, MSI and SSI standard cells. Our CAD tools are extremely advanced and user-friendly. Our software supports all of the major workstations: Daisy,™ Mentor,™ Valid,™ even the IBM PC.

With our small geometry CMOS technology, you can reduce an entire PC board of capability onto a single ASIC chip. You benefit with smaller power supplies, lower system cost, smaller system-level boards and higher system reliability.

Working through one of our design centers, you get fast, accurate service. Simulation and testability steps built into the design flow allow us to achieve almost 100% first time success.

Data base scaling upgrades without redesign.

Your design can take advantage of next generation I-micron CMOS geometries without redesign. So you'll sit back and watch your ASIC get faster all the time.

High Rel, too.

These standard cells are also characterized over the full military temperature range.

Choose your source and call today.

For more information, or to get started on your design, call your RCA or WSI sales office or design center today.

WaferScale Integration, Inc.

RCA

CIRCLE NO 88

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	5	16	63	16	0	0	7.9	7.2
Pot-Core	0	23	54	23	0	0	8.5	7.8
Laminate (power)	0	26	48	26	0	0	8.5	8.3
CONNECTORS								
Military panel	0	11	45	33	11	0	12.0	6.2
Flat/Cable	22	44	28	6	0	0	4.0	4.3
Multipin circular	0	33	42	25	0	0	8.0	8.1
PC	0	46	46	8	0	0	5.8	4.4
RF/Coaxial	7	43	21	29	0	0	7.1	5.6
Socket	23	59	9	9	0	0	3.4	3.5
Terminal blocks	11	39	33	17	0	0	6.1	4.5
Edge card	20	40	27	13	0	0	5.1	4.3
Subminiature	13	50	31	6	0	0	4.5	5.8
Rack & panel	11	33	45	11	0	0	6.0	5.6
Power	17	58	17	8	0	0	3.8	3.1
PRINTED CIRCUIT BOARDS								
Single-sided	0	71	29	0	0	0	3.7	4.1
Double-sided	0	44	56	0	0	0	5.4	5.0
Multilayer	0	25	69	6	0	0	7.0	5.7
Prototype	4	82	14	0	0	0	2.7	2.4
RESISTORS								
Carbon film	38	35	27	0	0	0	2.8	3.6
Carbon composition	30	30	31	9	0	0	4.4	4.3
Metal film	35	35	30	0	0	0	3.1	3.4
Metal oxide	30	20	40	10	0	0	5.2	4.2
Wirewound	19	24	48	9	0	0	5.8	4.9
Potentiometers	10	48	35	7	0	0	4.8	4.1
Networks	10	45	45	0	0	0	4.5	2.4
FUSES	46	18	36	0	0	0	3.3	3.1
SWITCHES								
Pushbutton	15	55	20	10	0	0	4.3	4.2
Rotary	20	47	20	13	0	0	4.7	7.4
Rocker	14	57	22	7	0	0	4.0	4.6
Thumbwheel	0	64	27	9	0	0	4.9	4.5
Snap action	15	46	23	16	0	0	5.2	4.9
Momentary	0	64	18	18	0	0	5.6	5.1
Dual in-line	8	50	25	17	0	0	5.7	4.4
WIRE AND CABLE								
Coaxial	33	47	20	0	0	0	2.5	1.9
Flat ribbon	32	47	21	0	0	0	2.6	2.6
Multiconductor	12	47	35	0	6	0	5.3	3.0
Hookup	59	33	8	0	0	0	1.3	1.4
Wire wrap	40	40	20	0	0	0	2.4	2.0
Power cords	19	43	29	9	0	0	4.7	4.6
Other	17	33	50	0	0	0	4.7	6.3
POWER SUPPLIES								
Switching	0	27	60	13	0	0	7.5	6.5
Linear	19	19	56	6	0	0	5.9	6.0
CIRCUIT BREAKERS	20	20	33	27	0	0	7.3	7.7
HEAT SINKS	14	48	33	5	0	0	4.4	4.7

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	33	17	39	11	0	0	5.2	5.4
PC board	0	33	33	34	0	0	8.7	7.5
Dry reed	0	29	71	0	0	0	6.3	6.7
Mercury	40	20	40	0	0	0	3.6	6.0
Solid state	15	31	31	23	0	0	6.8	8.3
DISCRETE SEMICONDUCTORS								
Diode	28	33	30	9	0	0	4.5	4.8
Zener	24	40	24	8	0	4	5.2	4.5
Thyristor	8	33	42	17	0	0	6.7	5.8
Small signal transistor	25	30	25	20	0	0	5.8	5.9
FET, MOS	23	23	23	31	0	0	7.2	7.3
Power, bipolar	17	42	25	16	0	0	5.5	7.5
INTEGRATED CIRCUITS, DIGITAL								
CMOS	8	42	33	17	0	0	6.2	5.8
TTL	10	40	40	10	0	0	5.6	6.2
LS	5	40	25	30	0	0	7.6	6.1
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	0	40	47	13	0	0	6.7	8.4
OP amplifier	10	32	42	16	0	0	6.5	7.0
Voltage regulator	10	45	30	15	0	0	5.7	6.4
MEMORY CIRCUITS								
RAM 16k	29	21	29	21	0	0	6.1	7.7
RAM 64k	21	36	36	7	0	0	4.7	8.7
RAM 256k	7	27	46	20	0	0	7.5	7.4
ROM/PROM	20	33	34	13	0	0	5.5	9.0
EPROM	14	29	38	19	0	0	6.7	5.9
EEPROM	18	27	37	18	0	0	6.4	7.9
DISPLAYS								
Panel meters	8	31	38	23	0	0	7.4	6.0
Fluorescent	13	25	37	25	0	0	7.5	11.4
Incandescent	11	56	22	11	0	0	4.7	7.8
LED	20	40	35	5	0	0	4.4	5.3
Liquid crystal	9	18	55	18	0	0	7.6	6.4
MICROPROCESSOR ICs								
8-bit	18	23	41	18	0	0	6.6	6.1
16-bit	14	29	50	7	0	0	5.7	6.9
FUNCTION PACKAGES								
Amplifier	9	46	27	18	0	0	6.0	8.2
Converter, analog to digital	8	42	25	25	0	0	6.8	7.4
Converter, digital to analog	0	46	27	27	0	0	7.5	8.4
LINE FILTERS	27	9	46	18	0	0	6.7	7.5
CAPACITORS								
Ceramic	26	31	35	8	0	0	4.6	3.9
Ceramic monolithic	21	33	33	13	0	0	5.3	4.1
Ceramic disc	29	25	38	8	0	0	4.8	4.9
Film	18	27	46	9	0	0	5.6	5.7
Electrolytic	23	23	42	12	0	0	5.7	6.7
Tantalum	21	25	50	4	0	0	5.1	6.0
INDUCTORS	20	33	40	7	0	0	4.9	6.1

Source: *Electronic Purchasing* magazine's survey of buyers

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MODEL BC200 SPECIFICATIONS

DIMENSIONS	**1.875" x 5.75" x 8"**
Input voltage	*22 to 32 V dc*
Outputs	*5 V, ±12 V; or 5 V, ±15 V*
Switching frequency	*100 kHz*
Efficiency	*60% minimum*
Ripple/noise	*100 mV peak-to-peak maximum*
Line regulation	*10 mV (22 to 32 V dc)*
Load regulation	*10 mV main (0.5% aux outputs)*
EMI	*Meets MIL-STD-461B*
Environment	*MIL-STD-810C, MIL-S-901C*
Input protection	*MIL-STD-704D*
Operating temperature range	*−55°C to +100°C*
Storage temperature range	*−65°C to +125°C*
MTBF (Ground benign)*	
Standard	*140,000 hours*
ER option	*1,100,000 hours*
MTBF (Air inhabited)*	
Standard	*23,000 hours*
ER option	*160,000 hours*

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CIRCLE NO 89

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uPD9201	Floppy Disk Interface
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uPD9306	Hard Disk Interface
3. Data Communications	
uPD7210	GPIB/Talker, Listener, Controller
uPD7201A	Multiprotocol Serial Controller
4. Digital Signal Processing	
uPD7720	General Purpose Digital Signal Processor
uPD77P20	EPROM version of 7720
5. Speech	
uPD7730	ADPCM speech encoder/decoder
uPD7756	ADPCM phoneme speech synthesizer
K-3	Speech recognition 3-chip set

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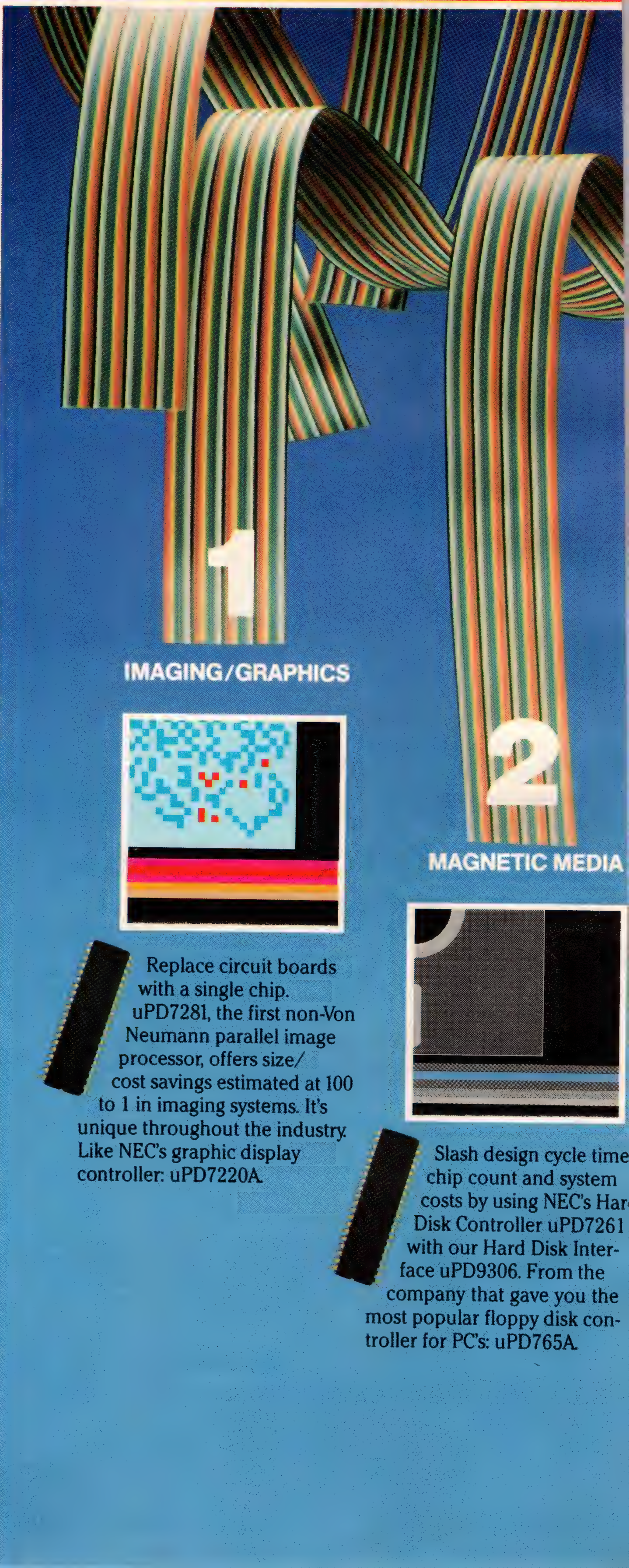

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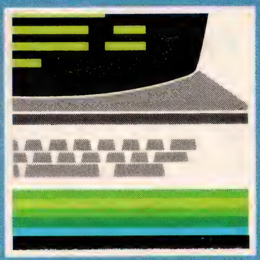

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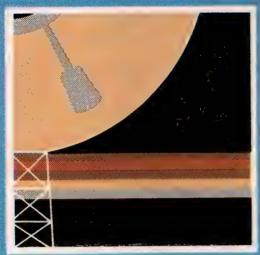

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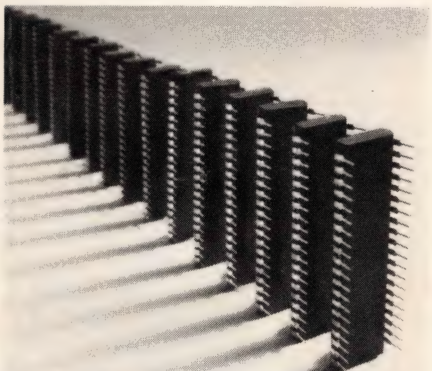

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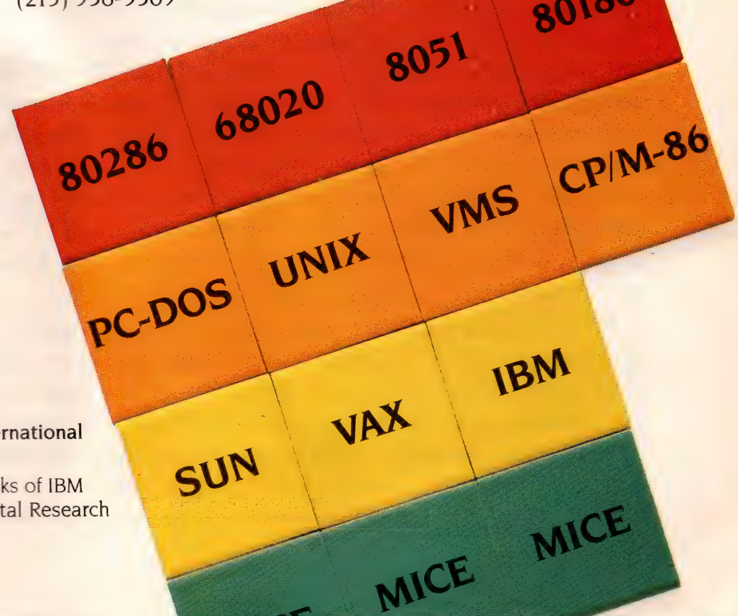

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CIRCLE NO 92

Analog-I/O boards and software for IBM PCs

Margery S Conner, *Regional Editor*

Software support for this year's wide variety of IBM PC analog-I/O boards ranges from terse machine-language drivers to general-purpose menu-driven packages. The software offered will suit almost any of your analog data-acquisition and -control applications for the PC.

When you're selecting a general-purpose analog-I/O board for your IBM PC or compatible computer, be sure to give equal attention to the software scheme you select. By making your hardware and software choice simultaneously, you'll be sure to choose the right board for your application and your level of programming skill.

You'll have a wide choice of both hardware and software this year. Manufacturers are offering many more boards than they did a year and a half ago. (Compare, for example, the boards discussed in **Ref 1** with those listed in the **tables** beginning on pg 126.) Moreover, the new boards offer higher throughput and more onboard functions (see **box,** "IBM PC add-in boards for analog I/O"), and several manufacturers include complete data-acquisition software packages with their products at no extra cost. What's more, third-party software vendors are offering off-the-shelf data-acquisition packages that run on a number of these boards, so for a given board, you can often choose from several software packages (see the **table,** pg 126).

Menu-driven software interfaces, whether from a third-party vendor or from a board manufacturer, are most useful to designers who have neither the time nor the inclination to become system experts in computer-based data acquisition. Such packages don't require the user to do any programming. Further, these off-the-shelf packages don't entail the expensive integration and debugging that user-written programs can require, and they don't carry the risk associated with custom programs.

If you're considering a menu-driven package, be aware that the capabilities of such packages vary widely. When you're evaluating the software, be sure to examine at least three factors: how well the package performs I/O functions, whether it can handle both acquisition and control (or only acquisition), and what its analysis and display capabilities are. Note also that off-the-shelf software packages won't suit every application. You might need to write your own software, for instance, if you're using a board whose I/O drivers are new or unsupported, or if your application is either a highly specialized one or a very simple one that doesn't warrant any extra expense.

Third-party software supports multiple boards

Because they can run on a number of boards from different manufacturers, third-party software packages may make it easier for you to find the right combination of hardware and software for your application. If you're considering a certain board, for example, you won't be limited to buying its manufacturer's

Continued on pg 120

PC add-in boards excel at analog-I/O tasks; *software packages simplify setup and control. (Photo courtesy Burr-Brown)*

Menu-driven software interfaces let you perform computer-based data acquisition without doing any programming.

IBM PC add-in boards for analog I/O

Recent efforts of companies offering analog-I/O add-ins for the IBM PC have engendered a wide selection of products that are faster than earlier models or that offer more functions—like DMA capability, or onboard data buffers, antialiasing filters, or μPs for signal processing. Other boards are notable for their low prices; you'll find ones costing as low as $169. If you can't find a standard board that cost-effectively suits your application, you can select a carrier board and populate it with plug-in modules to provide the I/O and conversion functions that you need.

Operating at 130k samples/sec for both A/D and D/A conversions, Data Translation's DT2821-F board transfers data to its host in 16-bit-wide samples, so you can use it only with the IBM PC/AT and compatibles. (The company offers slower boards for the IBM PC and PC/XT.) A RAM channel-gain list allows you to sample any of the channels at any gain and in any sequence at the full throughput rate. The board costs $1595 and is supported by the company's Atlab software package ($449), which is a library of subroutines for controlling all onboard digital and analog I/O functions. You can call the routines from Microsoft Fortran, C, and Pascal.

The Dash-16-AF ($1095) from Metrabyte features a different data-transfer method, which makes the board compatible with both the IBM PC/XT and PC/AT. The board performs DMA transfers of each sample in two 8-bit bytes. Therefore, the company claims, because the PC supports a DMA transfer rate of 250k bytes/sec, the board's sample-transfer rate is 125k 2-byte samples/sec. Nevertheless, the company rates the board conservatively at 100k samples/sec. Utility software, which comes with the board at no extra cost, consists of subroutines capable of controlling A/D- and D/A-channel functions; a graphics package for displaying processed data; and sample programs.

Antialiasing filters

Another board offering high-speed conversion is the A2D-160 from Microway. You can use the board to sample analog data, convert it, and write it to memory at speeds as high as 166k samples/sec in single-channel mode or 65k samples/sec in dual-channel mode. Memory transfer takes place via DMA; an onboard buffer prevents data loss when the PC's memory-segment boundaries are crossed. The A2D-160 offers optional antialiasing filters that are programmable for cutoff frequency, passband gain, and attenuation characteristics.

Dataq offers its WFS-200 waveform-display card with its Codas software package for $895 and adds a Metrabyte Dash-08 for an additional $395. The company will also provide the Dash-16 board. The combination offers 4k- or 5k-sample/sec real-time waveform display and storage to disk.

The company also offers an A/D-converter board, the DM-100PC ($575), which has programmable 12-, 16-, and 19-bit resolution modes. Option 01 ($175) lets you program any of the four channels for simultaneous acquisition of true-rms ac-voltage, dc-voltage, frequency, and resistance signals.

To maintain flexibility in configuring your system, you can plug a carrier board into your PC and add modules that supply only the I/O and conversion functions that you need. The advantage of this approach is that you have control over your board configuration; for example, you can provide more than 32 lines of digital I/O. Further, the configuration isn't fixed; you can replace the plug-ins later as your needs change. For a standard configuration, however, this plug-in approach is usually fairly expensive.

Carrier boards and modules are available from Qua Tech, Advanced Peripherals, ICS, and Burr-Brown. Burr-Brown's PCI-20041C-3 carrier board, for example, offers DMA transfer capability with a twist: Although

DMA transfers commonly handle only one type of data, such as outputs from an A/D converter, this board can transfer any combination of A/D, D/A, digital I/O, or clock/counter data. In addition to DMA, the board offers a pacer clock, 32 I/O lines, external interrupt capability, and a bus that allows data transfers between carrier boards. The PCI-20041C-2 offers the same features except for DMA. Each board can carry a maximum of three plug-in modules that supply A/D and D/A functions, as well as additional counter/timer and digital I/O functions.

Ultra-high-speed acquisition

Conventional DMA memory-transfer methods limit your sampling throughput to 250k to 350k bytes/sec. For higher speeds, you need a board that has buffer memory to store acquired data while the PC unloads it. This requirement limits you to using the board to acquire only small portions of a signal.

Among the boards that can perform such ultra-high-speed data acquisition are RC Electronics' IS-16 ($2495), which offers 0.01- to 1M-sample/sec throughput, and Integrated Systems Products' IS-2010 ($1500), which offers 25M-sample/sec performance. In addition, General Research's $2995 PCTR-160 digitizes at a 20M-sample/sec rate, but it controls trigger-to-sample times with sufficient accuracy to permit a 160M-sample/sec effective sampling rate for signals that repeat for eight trigger periods. With all three boards, software is included at no extra charge.

Onboard real-time processing

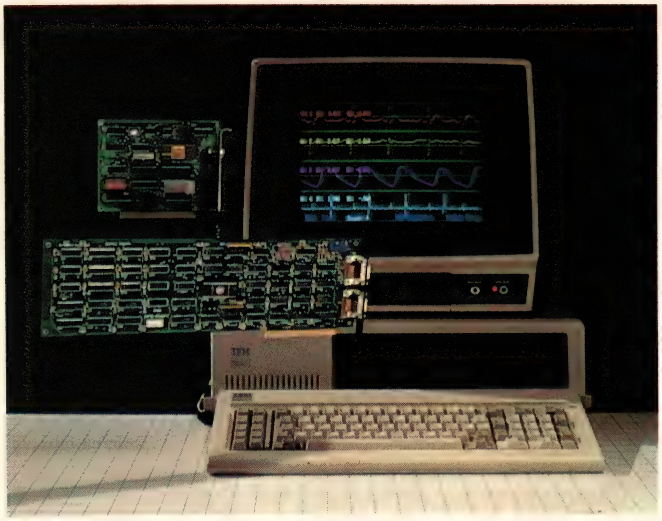
Other functions now available on analog-I/O boards include real-time processing. For example, Microstar Laboratories offers a board that employs an 8-MHz 80186 μP, 128k bytes of RAM, and a serial port to handle real-time processing of analog data. The board's data-acquisition circuitry includes a programmable-gain amplifier, dual S/H amplifiers, and a 16-bit A/D converter. The board's operating environment is configurable via Microstar's proprietary high-level language, DAPL. The PC and board processors communicate through Unix-like pipelines.

Because the board performs real-time processing of data, it can recognize a series of related events as meeting the criteria for a trigger. You can, therefore, examine signals characterized by criteria more complex than trigger presence and level. You can use the board to perform digital filtering of acquired data before passing it to the host.

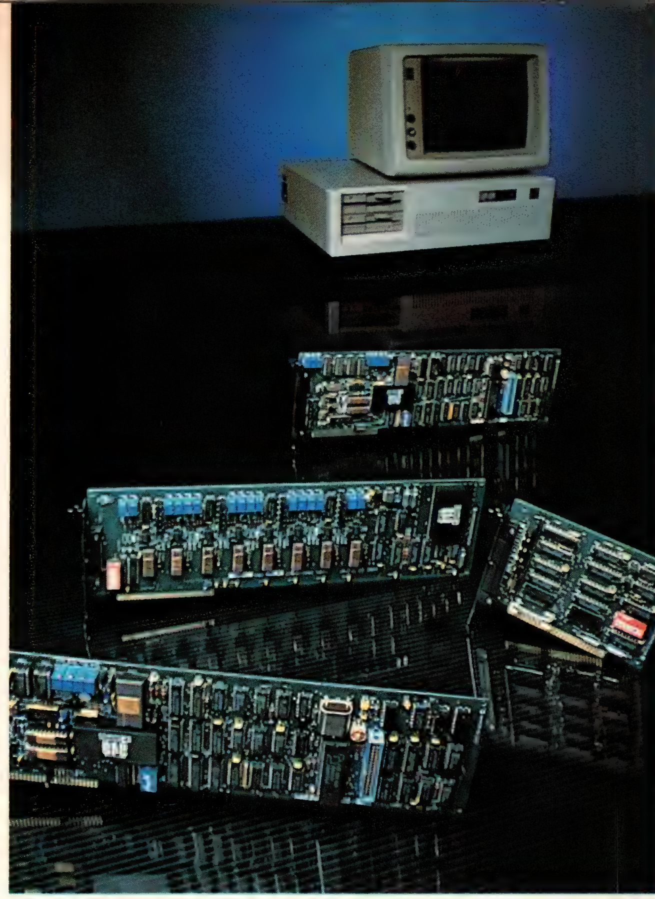
Boards priced less than $500 include the PCA/88 from Witt Engineering and Models 134 and 140 from Lawson Labs. The $169 PCA/88 features a single-channel 8-bit A/D converter with 66.7k-sample/sec throughput and jumper-selectable input ranges of 5 and 10V (bipolar and unipolar). An 8-bit D/A converter is also included.

Lawson Labs' Model 134 ($475) is a 4-channel, 16-bit successive-approximation A/D converter that's capable of 12k-sample/sec throughput at 16-bit resolution or 22k-sample/sec throughput at 8-bit resolution. The company's Model 140 ($265) offers four channels of 15-bit A/D resolution at 7.5 samples/sec. An optional differential multiplexer, Model 17B ($165), can add as many as 64 channels to the A/D converter. The boards come with the company's Fastsamp menu-driven software package. For sampling rates from 1k to 12k samples/sec, Fastsamp displays the sampling values on the screen and stores the data to disk. You can print a strip chart of the sampled waveform with an IBM graphics printer or a compatible machine. For rates below 1 sample/sec, you'll need the company's PC64 data-logging software ($150). You can call either of these packages from a user-written program.

Third-party software vendors are offering off-the-shelf data-acquisition packages that run on a number of boards from different manufacturers.



***A graphics accelerator card and software** make up Codas from Dataq Instruments. When you use Codas with a Dash-08 or Dash-16 card from Metrabyte, you can realize 5k-sample/sec real-time waveform display and storage to disk.*



***You can choose 32 single-ended or 16 differential channels** and realize a throughput of 71.4k samples/sec/channel by using a Series RTI-800 board from Analog Devices.*

proprietary software package, which might not suit your needs.

The third-party data-acquisition package that supports the largest number of boards is Laboratory Technologies' $895 Labtech Notebook. The program can display as many as 50 traces simultaneously in 15 windows; the number of traces it can actually acquire is limited only by your PC's memory. On PC/XT-based systems, the package can display 300 samples/sec in real time; on PC/AT-based systems, it can display 900 samples/sec in real time. At higher frequencies, the digitized information is first stored in RAM and then read from memory.

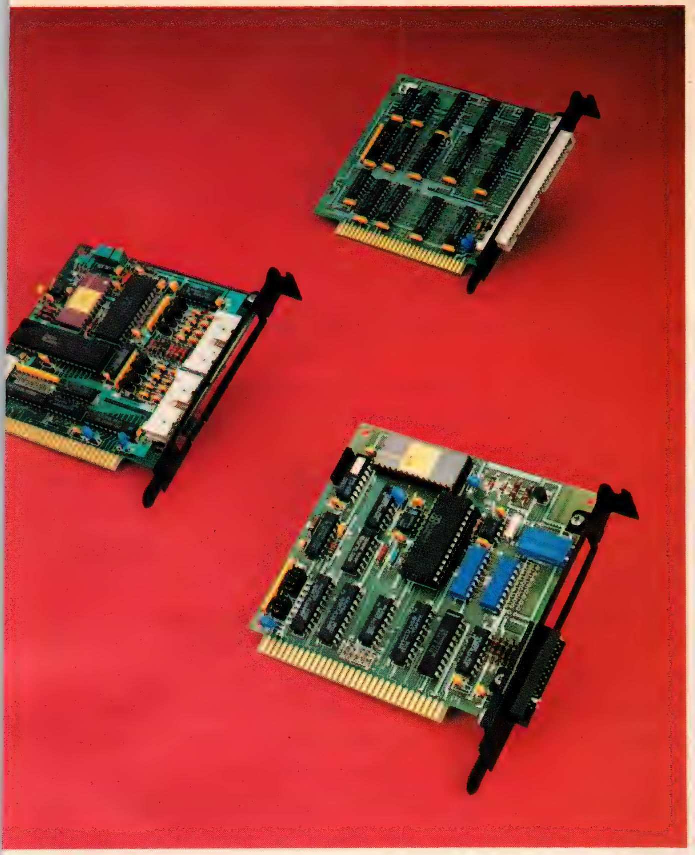
The package also offers two analytical routines: nonlinear curve-fitting routines, for as many as ten parameters, and fast Fourier transforms. Although these routines can take advantage of the 8087 floating-point processor, you don't have to have an 8087 to perform the routines. To perform additional analysis or any graphical display, however, you must purchase a separate spreadsheet program such as Lotus 1-2-3 from Lotus Development Corp (Cambridge, MA). Labtech Notebook's waveform data files are available in ASCII format for manipulation by a spreadsheet program.

Note, however, that although Lotus 1-2-3 is becoming something of a standard for post-acquisition analysis and graphics software, the spreadsheet was designed for business applications, and it's not optimized for engineering analysis. A spreadsheet that is optimized for engineering is RS/1 ($1900) from BBN Software. The package supports tabular manipulation of data, as does Lotus 1-2-3, but it also handles tasks like regression analysis, curve fitting, and graphical display, in either menu- or command-driven mode.

If you need to perform extensive statistical evaluation of your process or experiment, you can use a dedicated statistics package such as Northwest Analytical's Statpak ($495), which is tailored for probability calculation, single-variable statistical functions, regression and correlation, chi-square analysis, and the like.

Labtech Notebook is not limited to data acquisition; you can set all parameters needed for process-control modes, such as proportional-integral-derivation (PID), on/off (bang-bang), and alarm modes. Further, particularly when you're acquiring analog data at low rates (10 to 20 samples/sec), you can have the use of your PC by taking advantage of Labtech Notebook's foreground/background feature. You can make the acquisition function run in the background while you use the PC, say, as a word processor. Be aware, however, that because MS-DOS is not a multitasking operating system and Labtech Notebook uses a real-time clock, you can perform only certain kinds of tasks in the foreground. For example, if you format a disk—an operation that ties up the system clock—you risk aborting any task you're running in the background.

For simple data acquisition and display without analysis, you can use Snapshot Storage Scope ($495) from



For PCs that are tight on board space, *Data Translation offers three half-cards: the DT2814 analog-input card, the DT2815 analog-output card, and the DT2817 digital-I/O card.*

You can acquire data at 20M samples/sec *by using General Research's PC DAS, which combines the company's PCTR-160 board with menu-driven software.*

HEM Engineering. The package can display four of eight acquired channels, select a portion of the trace with two cursors, and display the differential time and voltage for either real-time or stored traces. The software also offers cursor scrolling.

Snapshot's setup screen gives you instant feedback on the parameters you select: It refuses to accept inconsistent combinations. When the program is in Replay mode, you can display signals stored on disk with the same parameters they were acquired with, because setup information is stored in the file along with the data points. The manufacturer offers FFT analysis as an option; for other analysis, you must purchase a spreadsheet program.

Perform signal analysis without a spreadsheet

Not all data-acquisition packages require you to purchase a separate spreadsheet to perform signal and graphical analysis and display, however. Some packages offer specialized analytical capabilities. Unkelscope from Unkel Software, for instance, is a menu-driven package that's capable of deriving a signal's FFT power spectral density and of performing integration; differentiation; and common functions such as log, square, square root, and exponentiation.

Unkelscope can also perform highpass, lowpass, and bandpass digital filtering. It lets you display two channels of acquired data in real time at rates to 20 samples/sec. After the data is displayed, you can use the cursor-scrolling feature to position the cursor anywhere on the trace and find the value of an individual data point. Further, the package doesn't limit you to signal-vs-time displays; you can also choose signal-vs-signal displays.

Another package that offers specialized analytical capabilities is Macmillan Software's Asystant+. This menu-driven package provides many of the features of the company's Asyst package (a number-crunching data-acquisition tool), but Asystant+ doesn't require that you learn the command set. Asystant+ is also one of the easiest menu-driven programs to configure: You select from five modes (the company calls them "metaphors") that you want the acquisition setup to simulate: strip-chart-recorder mode, transient-recorder mode, XY-recorder mode, data-logger mode, and high-speed-recorder mode. Each mode has its own menu.

When your files of acquired data are too large to be manipulated in memory, you can invoke the program's file processor. This processor can bring a portion of a file into memory, manipulate it in accordance with some user-defined procedure, such as a transformation or convolution, and then store the results in an output file. The interactive wave processor supports waveform display: You can select all or a portion of a trace; multiply, offset, filter, or reduce the trace; and overlay the new trace on the original.

Asystant+ displays data in real time at rates as high as 72 samples/sec on a 6-MHz PC/AT. In the high-speed

With some software packages, you must purchase a separate spreadsheet program to perform specialized analysis functions.

mode, the program can display 16 channels after capture. Using Dataq's high-speed scroller board ($895), you can display data from as many as four channels in real time at 800 samples/sec.

Perform real-time data manipulation

To perform extensive real-time manipulation of data on the screen, you can use a program like QED by Hart Scientific. That program offers integration and differentiation, scaling, addition of two traces, offset, and signal-range tracking. In post-acquisition mode, you can perform all these data-manipulation functions, as well as polynomial-curve and least-square fitting functions. For further analysis and display, you can use a spreadsheet program.

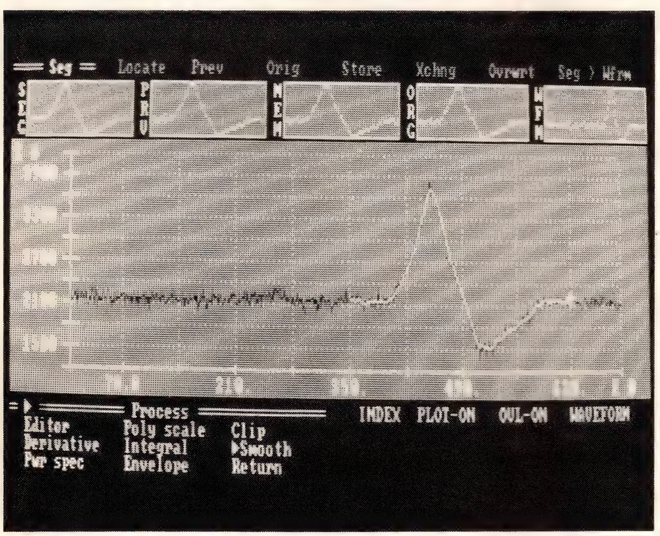
Another acquisition package, Cyborg's Discovery, is useful as a preprocessor. The software can acquire data and perform data-reduction operations such as finding Δx and Δy, the slope at any point, minimums and maximums, and the area under the curve. Reduced data is then accessible in ASCII format by a spreadsheet program.

RTSS from Data Motion combines the easy setup features of a conventional menu-driven package with pop-up spreadsheet convenience. The pop-up feature is especially useful when you want to monitor an ongoing data-acquisition task in the background without exiting your foreground program. You can set up the acquisition parameters from the popped-up menu, begin the acquisition or set a time delay, and then run another program while the data-acquisition task continues in background. At any time in the acquisition process you can pop up RTSS—without exiting your foreground program—and display a graph of your acquisition. Although the menu doesn't offer any predefined filter or analysis routines, you can define such routines by entering an equation in the appropriate spreadsheet cell.

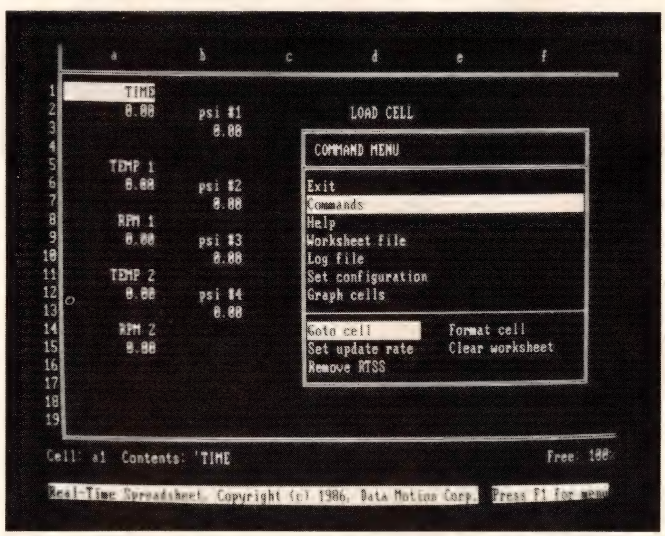
If your data-acquisition system doesn't require real-time response and real-time waveform display, consider buying a package like Signal Technology's ILS. Although it supports A/D and D/A functions, ILS primarily performs post-acquisition signal processing and analysis. After acquiring a waveform, you can use ILS to design a digital filter to your specifications, then simulate and display the effect of that filter on the acquired data. The software supports elliptic, Chebyshev, and Butterworth filter designs and simulations.

The package can help you perform spectral analysis of a signal by displaying the signal's Cepstrum and log-magnitude spectrum. Although it's not a menu-driven program in the conventional sense—that is, it doesn't limit your responses as menus do—the program guides you in selecting arguments for the command processor. When you become familiar with the program, you'll be able to use faster and more brief commands.

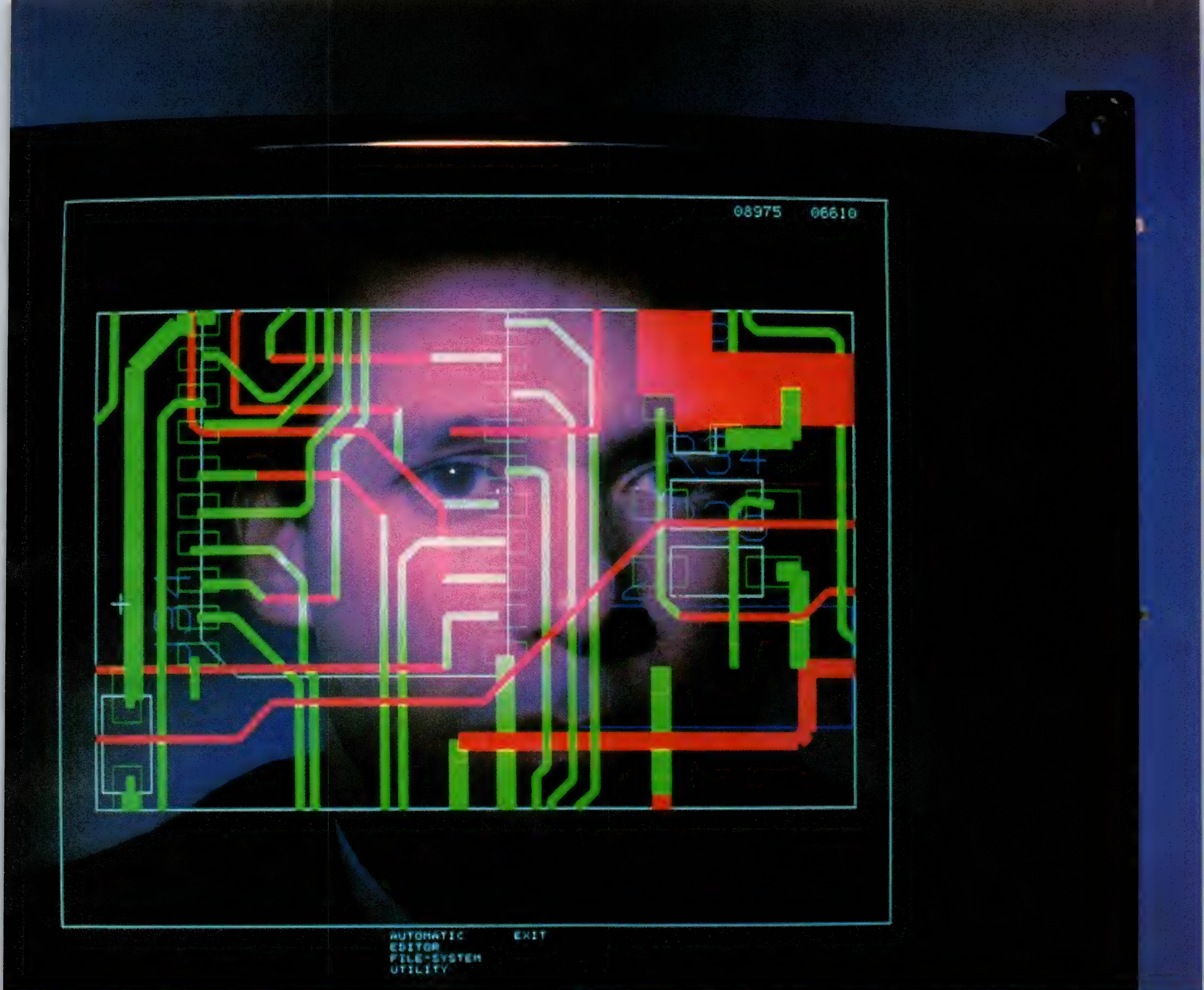
Continued on pg 126



For data reduction and analysis, *the interactive wave processor of Macmillan's Asystant+ can act as a visual calculator. Each small window represents a signal in memory. The large display shows a raw signal overlaid with its lowpass-filtered version.*



You can overlay command and help menus on a real-time data display *by using RTSS from Data Motion. While running another program in the foreground, you can pop up the RTSS data display at any time to set up and monitor data acquisition.*



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CIRCLE NO 93

Manufacturers of analog-I/O boards and software for the IBM PC

For more information on analog-I/O add-ins and software for the IBM PC, contact the following manufacturers directly or circle the appropriate numbers on the Information Retreival Service card.

Action Instruments Inc
8601 Aero Dr
San Diego, CA 92123
(619) 279-5726
Circle No 651

Advanced Peripherals Inc
12650 W Geauga Plaza
Chesterland, OH 44026
(216) 729-3927
Circle No 652

Analog Devices
Two Technology Way
Norwood, MA 02062
(617) 329-4700
Circle No 653

Anasco
Audubon Rd
Wakefield, MA 01880
(617) 246-0300
Circle No 654

Argis Inc
Box 373
Hudson, MA 01749
(617) 562-9673
Circle No 655

BBN Software Products Corp
10 Fawcett St
Cambridge, MA 02238
(617) 864-1780
Circle No 656

Burr-Brown
Box 11400
Tucson, AZ 85734
(602) 746-1111
Circle No 657

Cyborg Corp
55 Chapel St
Newton, MA 02158
(617) 964-9020
Circle No 658

Data Motion
Box 889
Orland Park, IL 60642
(312) 495-4007
Circle No 659

Data Translation Inc
100 Locke Dr
Marlboro, MA 01752
(617) 481-3700
Circle No 660

Dataq Instruments Inc
100 Lincoln St
Akron, OH 44308
(216) 434-4284
Circle No 661

General Research Corp
7655 Old Springhouse Rd
McLean, VA 22102
(703) 893-5900
Circle No 662

Gould Inc
Recording Systems Div
3631 Perkins Ave
Cleveland, OH 44114
(216) 361-3315
Circle No 663

HEM Engineering Co
17025 Crescent Dr
Southfield, MI 48076
(313) 559-5607
Circle No 664

Hamilton/HGL Software
6 Pearl Ct
Allendale, NJ 07401
(201) 327-1444
Circle No 665

Hart Scientific
177 W 300 South
Provo, UT 84601
(801) 375-7221
Circle No 666

ICS
8601 Aero Dr
San Diego, CA 92123
(619) 279-0084
Circle No 667

Integrated Systems Products Inc
6028 Fremont Circle
Camarillo, CA 93010
(805) 987-5125
Circle No 668

Interactive Microware Inc
Box 139
State College, PA 16804
(814) 238-8294
Circle No 669

Interactive Structures Inc
218 Great Valley Parkway
Malvern, PA 19355
(215) 644-8877
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Laboratory Technologies Corp
255 Ballardvale St
Wilmington, MA 01887
(617) 657-5400
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Lawson Labs Inc
5700 Raibe Rd
Columbia Falls, MT 59912
(406) 387-5355
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Macmillan Software Co
866 Third Ave
New York, NY 10022
(212) 702-3241
Circle No 673

Metrabyte Corp
440 Myles Standish Rd
Taunton, MA 02780
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Circle No 674

Microcomputer Systems Inc
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Baton Rouge, LA 70808
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Microstar Laboratories Inc
2863 152 Ave NE
Redmond, WA 98052
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Microway Inc
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Kingston, MA 02364
(617) 746-7341
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Northwest Analytical Inc
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Portland, OR 97209
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Qua Tech Inc
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Akron, OH 44304
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RC Electronics Inc
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Santa Barbara, CA 93111
(805) 964-6708
Circle No 680

Scientific Solutions Inc
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Solon, OH 44139
(216) 349-4030
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Signal Technology Inc
5951 Encina Rd
Goleta, CA 93117
(805) 683-3771
Circle No 682

Strawberry Tree Computers
1010 W Fremont Ave
Sunnyvale, CA 94087
(408) 736-3083
Circle No 683

Taurus Computer Products Inc
1755 Woodward Dr
Ottawa, Ontario K2C 0P9, Canada
(613) 226-5361
Circle No 684

Unkel Software Inc
62 Bridge St
Lexington, MA 02173
(617) 861-0181
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Witt Engineering
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Glenview, IL 60025
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Several board manufacturers include complete data-acquisition software packages with their products at no extra charge.

Also targeting frequency- and time-domain analysis is DATS from Hamilton/HGL Software. The package, which has extensive statistical-analysis capabilities, can perform both data acquisition and post processing. You can access the program from the menu-driven or command-driven modes, or you can invoke individual modules from Fortran. DATS requires a coprocessor because of the extensive computational tasks it performs, and the vendor recommends that you run the program on a PC/AT or compatible machine.

Several hardware manufacturers offer menu-driven software specific to their board lines. Some of these packages can cost as much as several thousand dollars; others come with the boards at no additional cost. Strawberry Tree Computers, for example, offers a menu-driven package whose price is included in the basic prices of the company's $640 to $1590 Analog Connection boards. Offering the traditional menu-driven features of channel setup, waveform display, and data logging, the package also comes with Basic source code, so you can customize it. The package's I/O drivers are written in machine language for faster execution.

A much more complex package, the DASA menu-driven package from Gould's Recording Systems Div, costs $4000. The package, which supports the company's DASA 4600 board, comprises three modules that handle menu/DOS interfacing; the display, annotation, and output of acquired data; and channel setup. Gould's DASA 4600 board features a 50k-sample/sec sampling rate, 40k-sample/sec logging to disk, 12-bit resolution, and a constant 20-μsec skew on the channel selection to maintain a time relationship between channels. The board's price includes I/O drivers. If you want cursor-scrolling capability, you can purchase the company's

THIRD-PARTY SOFTWARE PACKAGES FOR ANALOG-I/O PC ADD-INS

PACKAGE/COMPANY	8087 SUPPORT	NUMBER OF CHANNELS	ANALYTICAL ROUTINES	FOREGROUND/ BACKGROUND CAPABILITY	TIME STAMP	CURSOR SCROLLING
ASYSTANT + MACMILLAN SOFTWARE	•	16	ALL		•	•
DATS/ HAMILTON/HGL	•	16	ALL			•
DISCOVERY/ CYBORG	8087	100	FFT, CROSS- AND AUTO CORRELATION		•	•
ILS/ SIGNAL TECHNOLOGY	•	HARDWARE LIMITED	ALL			•
LABTECH NOTEBOOK/ LABORATORY TECHNOLOGIES	•	HARDWARE LIMITED	FFT, CURVE FITS	•	•	
QED/ HART SCIENTIFIC	•	HARDWARE LIMITED	CURVE FITS, STATISTICAL ANALYSIS	•		
RTSS/ DATA MOTION	•	1	USER-PROGRAMMED	•		
SNAPSHOT STORAGE SCOPE/ HEM ENGINEERING		4	FFT (OPTIONAL)		•	•
UNKELSCOPE/ UNKEL SOFTWARE	•	9	FFT, CURVE FITS, COMMON TRANSFORMS		•	•

*PROPORTIONAL INTEGRAL DERIVATION

$1000 waveform-scroller board.

Also offering you a choice of software support are the RTI-800 Series boards from Analog Devices. The basic PC-DOS driver package ($195) includes drivers for Fortran, Basic, and C. The $295 Turbo Pascal package includes both the I/O drivers and Turbo Lablog, a menu-driven application package. Lablog allows you to modify all system parameters (such as alarm limits, scan rates, and channel settings) on the fly. It supports real-time graphics and data logging to disk.

For ordinary data-acquisition and -control applications, you can use Burr-Brown's Controlograph data-logger software ($850), which runs on the company's PCI 20000 data-acquisition boards. The package supports channel and trigger setup, real-time display, data logging to disk, and graphing. You can use a spreadsheet such as Lotus 1-2-3 for analysis. **EDN**

References

1. Travis, Bill, "Analog-input and -output plug-in boards mate IBM PC and clones to real world," *EDN*, November 15, 1984, pg 53.

2. Schreier, Paul G, "Next-generation I/O software requires minimal programming," *EDN*, December 13, 1984, pg 284.

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

REAL-TIME DISPLAY	PROCESS CONTROL	SIGNAL VS SIGNAL DISPLAY	SOFTWARE FILTER	COMPARES REAL-TIME DATA TO STORED DATA	PROGRAMMING OPTION	TABULAR DISPLAY	PRICE	COPY PROTECTION
•	ALARM	•	•	•	•	•	$ 895	•
		•	•	•	•	•	$2500	
•			•		•	•	$1195	
•	•	•	•			•	$1495	HARDWARE PROTECTION
•	PID*, ON-OFF, ALARM	•		•	•	•	$ 895	•
•	ALARM	•	•	•	•		$ 849	
•		•			•	•	$ 345	UNPROTECTED VERSION COSTS $50 MORE
•						•	$ 495	
•	PID*, ON-OFF	•	•	•	•		$ 549	

Table continued on pg 130

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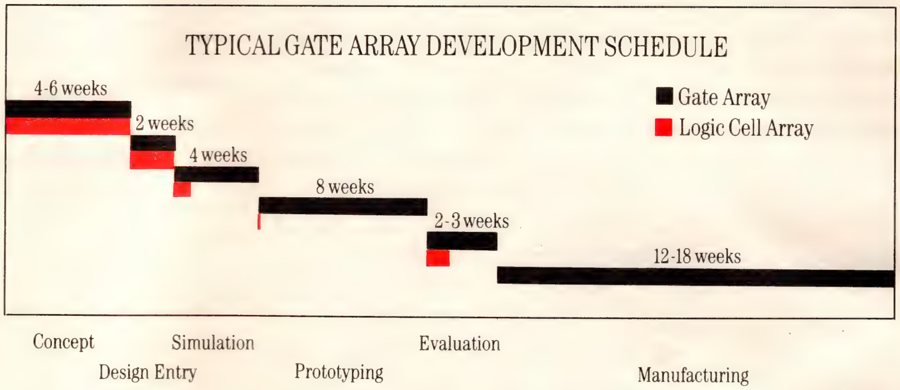
A PROGRAMMA

You've known it all along.

Now, the ideal logic device is finally here: Real gate array density. Real gate array architecture. Real gate array flexibility. And fully user programmable.

It's called the Logic Cell™ Array and it's from Xilinx.



Since you program it yourself, the Logic Cell Array shortens design verification and prototyping to almost nothing, and completely eliminates manufacturing. That cuts about 5½ months out of the typical schedule. And that's just on the first go-round. If you have to change the Logic Cell Array, all you do is reprogram it. That could take you a whole afternoon.

A GATE ARRAY. ONLY BETTER.

The Logic Cell Array offers all the advantages—but none of the disadvantages—of conventional gate arrays. Unlike them, the Logic Cell Array isn't manufactured. Merely programmed. And it can be reprogrammed an unlimited number of times. Even while it's in the system.

That means turnaround time on design revs can be measured in hours, not months. Time-to-market can be reduced accordingly. And non-recurring engineering charges are non-existent.

Logic Cell Arrays are also standard parts. So we can test every one of them 100%, down to the last transistor, before you ever get them.

It also means that, unlike gate arrays, you can get Logic Cell Arrays off-the-shelf, through distribution.

The specs on this little silicon gem?

Part No. XC-2064. CMOS. 40 MHz. And 1200 honest, usable gates. Look for 3000 gates by year-end.

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The problem with logic devices, gate arrays in particular, is they're hard-wired. So your design is literally cast in silicon.

It might as well be cast in cement.

Imagine, though, how much simpler your life would be if your logic device had the flexibility of

With the Logic Cell Array's real time in-ciruit emulation, you get 100% design verification, in the system. It's the real thing. The best you can do with a gate array is simu lation. Which is about as close to the real thing as a decoy is to a real duck. So how can you really be sure your design is going to fly?

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URSE.
BLE GATE ARRAY.

a microprocessor. Well, the Logic Cell Array has that flexibility. Because it works very much like a microprocessor.

At power up, the Logic Cell Array automatically loads its internal CMOS static memory. This memory defines the logic functions and interconnections within the Logic Cell Array to build your logic circuit.

As for the advantages of such an approach, just go ask the microprocessor guys.

As for the advantages of being based on CMOS memory, talk to those who work with memory about how much they like parts that continually drop in price while increasing in density and performance.

Because the Logic Cell Array is going to do that, too.

A FULL ARRAY OF DEVELOPMENT SYSTEM SUPPORT.

You don't have to be an expert in semiconductor manufacturing to use the Logic Cell Array. You just have to know logic design.

And you don't have to be a programming expert to use any part of our integrated development system, either.

There's an interactive, graphics-based, mouse-and-menu-driven configuration editor that you can learn in an afternoon.

Instead of a lot of gate arrays that each do one thing, the Logic Cell Array is one gate array that can do everything. Including cut your inventory risk to zero, let you make field upgrades, and eliminate NRE.

A simulator. An in-circuit emulator that runs real I/O and real software in real time for complete and positive design verification.

Plus documentation at the touch of a button and host of other why-didn't-somebody-think-of-that-before facilities.

Best of all, it runs on an IBM® PC XT,™ AT™ or clone. And you can get started for the modest price of just $3600.

TRY IT. $250.

We've arranged a way for you to find out firsthand what you can do with the Logic Cell Array. It's our Evaluation Kit (otherwise known as EK-01). And it's just $250.

It includes enough software and documentation to evaluate your application on a Logic Cell Array, and see if it performs up to snuff. If you decide the Logic Cell Array is just what you need, we'll credit your $250 towards the purchase of our XACT™ development system.

To order, call Hamilton/Avnet toll-free at 1-800-4-HAMILTON. Or contact your local Xilinx sales office or Xilinx representative.

Immediately, if not sooner.

Now that the ideal logic device is here, isn't this the ideal time to use it?

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CIRCLE NO 95

ANALOG I/O ADD-IN BOARDS FOR IBM PCs AND COMPATIBLES

MANUFACTURER	BOARD	A/D CHANNELS	A/D RESOLUTION (BITS)	THROUGHPUT (SAMPLES/ SEC)	A/D RANGES (V)	A/D RANGE SELECTION	PROGRAM-MABLE GAIN	PROGRAM-MING METHOD
ACTION INSTRUMENTS	AI04	4 DI	12	30	±2	—	1, 100, 1000	SWITCHES
	AI08	8 SE	12	25k	±5	—	—	—
	AI016	16 SE, 8 DI	12	40k	±10	—	0.5, 1, 2, 5, 10	SWITCHES
ADVANCED PERIPHERALS	MIDAS SYSTEM C100**	8 DI	15	10	FACTORY-SET	—	—	—
ANALOG DEVICES	RTI-800	16 SE, 8 DI	12	32.2k	0 TO 10, ±5, ±10	JUMPER	1, 10, 100, 500	SOFTWARE
	RTI-815	16 SE, 8 DI	12	32.2k	0 TO 10, ±5, ±10	JUMPER	1, 10, 100, 500	SOFTWARE
	RTI-802-4	—	—	—	—	—	—	—
	RTI-802-8	—	—	—	—	—	—	—
ANASCO	41-401	16 SE, 8 DI	12	50k	±0.5, ±1, ±2.5, ±5, ±10, 0 TO 1, 0 TO 2, 0 TO 5, 0 TO 10	SWITCH	0.5, 1, 2, 5, 10	SWITCH
	41-402	8 SE	12	30k	±5	SWITCH	—	—
BURR-BROWN	PCI-20041C-3 CARRIER BOARD**	16 SE, 8 DI	12	32k OR 89k	±5, ±10, 0 TO 10; OR 0 TO 5, 0 TO 10, ±2.5, ±5, ±10	JUMPER	1, 10, 100, 1000	SOFTWARE
DATA TRANSLATION	DT2801 FAMILY	8 DI OR 16 SE, 8 DI	12 OR 16	2.5k, 13.7k, OR 27.5k	0 TO 5, 0 TO 10; OR 0 TO 1.25, 0 TO 2.5, ±1.25, ±2.5, ±5, ±10	JUMPERS	1, 2, 4, 8	SOFTWARE
	DT2805 AND DT2805/5716	8 DI	12 OR 16	2.5k OR 13.7k	0 TO 5, 0 TO 10; OR 0 TO 1.25, 0 TO 2.5, ±1.25, ±2.5, ±5, ±10	JUMPERS	1, 10, 100, 500	SOFTWARE
	DT2808	16 SE	10	3k	0 TO 5	—	—	—
	DT2818	4 SE	12	27.5k	0 TO 10, ±10	JUMPERS	—	—

*PROGRAMMABLE
**CARRIER BOARD AND MODULES

L = LABTECH NOTEBOOK
U = UNKELSCOPE
R = RTSS
C = CODAS
Q = QED
S = SNAPSHOT
A = ASYSTANT+
I = ILS
SE = SINGLE-ENDED
DI = DIFFERENTIAL

D/A CHANNELS	D/A RESOLUTION (BITS)	D/A RANGES (V)	DIGITAL I/O LINES	CLOCK/ COUNTERS	PRICE	VENDOR SOFTWARE SUPPORT	THIRD-PARTY SOFTWARE SUPPORT	COMMENTS
2	12	0 TO 5, 0 TO 10, ±2.5, ±5, ±10	12	—	$ 850	I/O DRIVERS, SAMPLE PROGRAM INCLUDED	L	2 CHANNELS CAN BE USED AS RTD (RESISTANCE-TEMPERATURE-DEVICE) INPUT
—	—	—	7	—	$ 695	I/O DRIVERS, SAMPLE PROGRAM INCLUDED	L, U	
2	8	0 TO 5	8	3 16-BIT COUNTERS	$1225	I/O DRIVERS, SAMPLE PROGRAM INCLUDED	L, U	
2	12	FACTORY-SET	8	4 COUNTERS	$ 760	I/O DRIVERS INCLUDED	L	CARRIER BOARD REQUIRES FROM 1 TO 3 MODULES. MODULES COST FROM $495 TO $600; SPECS DEPEND ON MODULES
—	—	—	8	16-BIT PACER CLOCK	$ 850	DRIVERS IN BASIC, C, FORTRAN, $195; LABLOG, $295	L, Q, U, A, S	OA-10 OPTIONAL EXPANDER OFFERS 32 SE, 16 DI CHANNELS; 3 COUNTER/TIMER CHANNELS; 4-BIT FREQUENCY-OUTPUT CHANNELS; AND 71.4-kHz THROUGHPUT
2	12	0 TO 10, ±10	8	16-BIT PACER CLOCK	$1095	DRIVERS IN BASIC, C, FORTRAN, $195; LABLOG, $295	L, Q, U, A, S	OA-10 OPTIONAL EXPANDER OFFERS 32 SE, 16 DI CHANNELS; 3 COUNTER/TIMER CHANNELS; 4-BIT FREQUENCY-OUTPUT CHANNELS; AND 71.4-kHz THROUGHPUT
4	12	0 TO 10, ±10	—	—	$ 695	DRIVERS IN BASIC, C, FORTRAN, $195; LABLOG, $295	—	
8	12	0 TO 10, ±10	—	—	$1095	DRIVERS IN BASIC, C, FORTRAN, $195; LABLOG, $295	—	
2	12	0 TO 5	8	PROGRAMMABLE TIMER	$1025	I/O DRIVERS INCLUDED	L, S	
—	—	—	7	PROGRAMMABLE TIMER	$ 435	I/O DRIVERS INCLUDED	L, S	
1, 2, OR 8	12 OR 16	0 TO 10 OR ±5 AND ±10	32	PROGRAMMABLE 8-MHz CLOCK	$ 695	SUBROUTINE PACKAGE, $250; CONTROLOGRAPH, $850	L	CARRIER BOARD REQUIRES FROM 1 TO 3 MODULES. SPECS DEPEND ON MODULES, WHICH COST FROM $229 TO $598
2	12	0 TO 5, 0 TO 10, ±2.5, ±5, ±10	16	400- OR 800-kHz CLOCK	$ 995 TO $1970	PC LAB SUBROUTINES, $249	L, U, Q, R, S, A	FAMILY INCLUDES DT2801, DT2801A, DT2801/5714, AND DT2801/5716. SPECS AND PRICES DEPEND ON MODEL
2	12	0 TO 5, 0 TO 10, ±2, ±5, ±10	16	400-Hz CLOCK	$1095 OR $2070	PC LAB SUBROUTINES, $249	L, A, S, R, I	A/D CHANNELS, THROUGHPUT, AND PRICE DEPEND ON MODEL
2	8	0 TO 5, ±5	16	5 μSEC TO 0.1638 SEC IN 2.5-μSEC INCREMENTS	$ 495	PC LAB SUBROUTINES, $249	L, A, S, I	
2	12	0 TO 5, 0 TO 10, ±5, ±10	16	2.5 μSEC TO 0.089 SEC IN 1.25-μSEC INCREMENTS	$1695	PC LAB SUBROUTINES, $249	L, S, U, I	SIMULTANEOUS S/H CAPABILITY; ACQUIRES 4 CHANNELS AT ONE TIME

Table continued on pg 134

SIEMENS

A jump ahead in quality. Longterm failure rate 2 fit. Siemens of course.

To be ahead in electronic components you need to have your nose in front when it comes to product quality. Testing at extremes of heat and cold helps guarantee it. And a major criterion in judging quality is longterm failure rate, like the 2 fit that Siemens achieves with its capacitors.

Delivery quality is exemplary too, with "defects" of 0.007% on passive components. And equally important: a wide variety of passive components meet demanding CECC qualification.

Quality produced by 27,000 employees, with thousands of million marks going into R&D annually. That's what Siemens customers can bank on, worldwide.

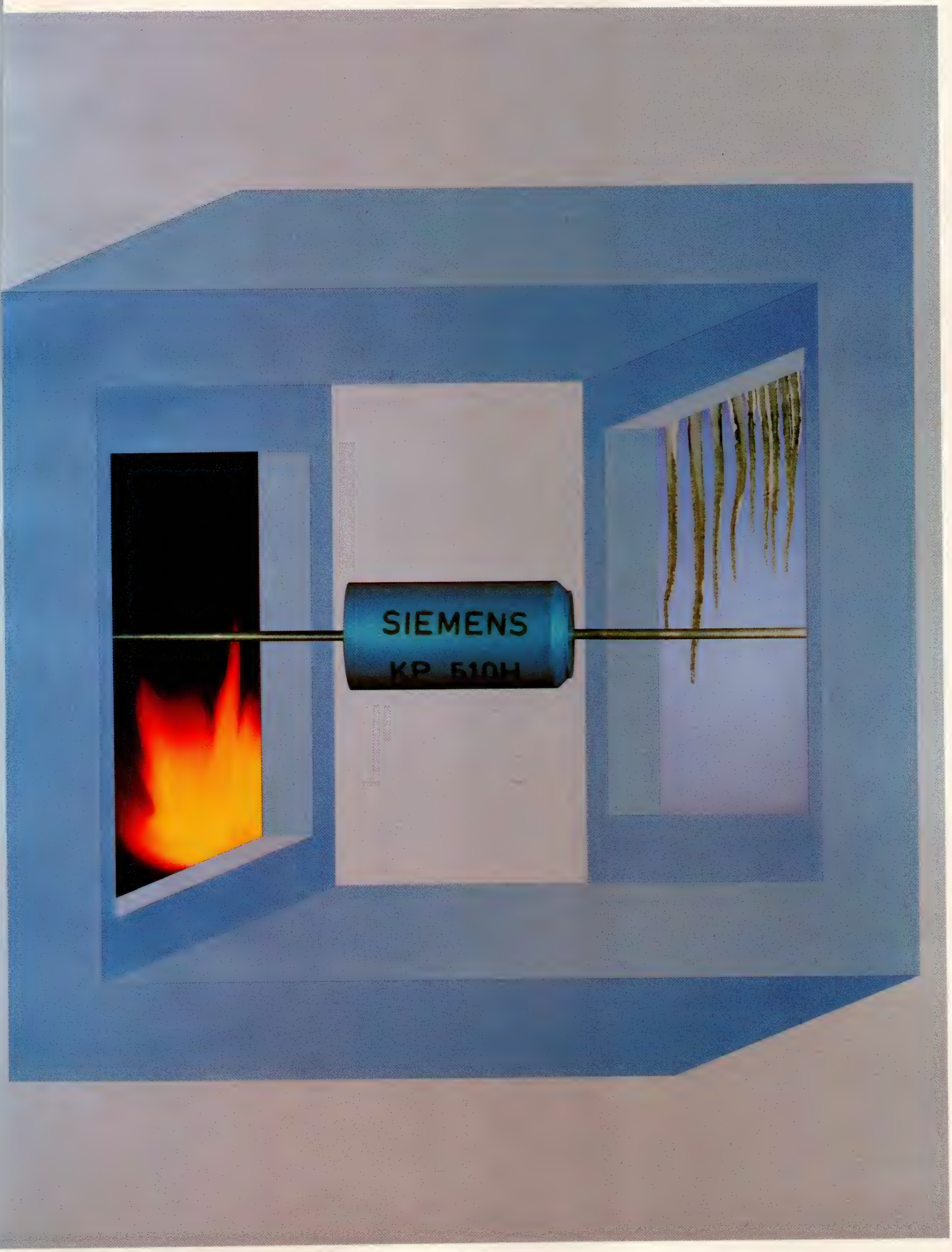
Everything it takes in electronics. Siemens.

Not only product quality has to be right, the quality of service must be on the mark too. Dependability in delivery and on deadlines, flexibility, comprehensive documentation are just as important when you're a Siemens customer.

Example: in the assessment of big customers Siemens regularly comes away with a rating of 100% on serviceability, which often means satisfying more than ten different criteria.

Siemens controls the reliability of its components through periodic environmental and longterm tests.

Example: each capacitor is tested 100% to specification.



Component quality also means using the experience fed back from applications. And here Siemens can draw from the know-how of its system experience.

Siemens AG, Components Group, Balanstrasse 73, 8000 Munich 80, West Germany.

12/Z009e

ANALOG I/O ADD-IN BOARDS FOR IBM PCs AND COMPATIBLES *(Continued)*

MANUFACTURER	BOARD	A/D CHANNELS	A/D RESOLUTION (BITS)	THROUGHPUT (SAMPLES/SEC)	A/D RANGES (V)	A/D RANGE SELECTION	PROGRAMMABLE GAIN	PROGRAMMING METHOD
DATA TRANSLATION (Continued)	DT2806** CARRIER BOARD	64 SE OR 32 DI	12	20k	0 TO 5, ±2.5, ±5	JUMPER	1, 10, 100, 1000	RESISTOR
	DT2814	16	12	30k	±5	—	—	—
	DT2815	—	—	—	—	—	—	—
	DT2821 AND DT2821-F	16 SE, 8 DI	12	50k OR 130k	0 TO 10, ±10	JUMPER	1, 2, 4, 8	SOFTWARE
	DT2827	4 DI	16	100k	±10	JUMPER	—	—
	DT2828	4 SE	12	100k	0 TO 10, ±10	JUMPER	—	—
DATAQ INSTRUMENTS	DM-100PC	4	19 MAX*	33	±3.3, ±30, ±300	SOFTWARE	—	—
GOULD RECORDING SYSTEMS DIV	DASA 4600	16 SE	12	40k	0 TO 1, 0 TO 2, 0 TO 5, 0 TO 10, ±0.5, ±1, ±5, ±10	SWITCH	—	—
ICS	ICS541	16 SE, 8 DI	12 OR 13	10 OR 50k	±10	—	1 TO 2048 IN 12 STEPS	SOFTWARE
INTERACTIVE MICROWARE	ADALAB-PC	4 DI (8 OR 16 DI OPTIONAL)	12	30 (20k OPTIONAL)	±4, ±2.5, ±1, ±0.5, ±5, ±10, 0 TO 10	JUMPER	1 TO 256 OPTIONAL	SOFTWARE
INTERACTIVE STRUCTURES	DAISI SYSTEM**	16 PER MODULE	12	64.5k (10.7k WORST CASE)	−5 TO +5, −1 TO +1, −0.5 TO +0.5, −0.1 TO +0.1, 0 TO 5, 0 TO 1, 0 TO 0.1, 0 TO 0.5	SOFTWARE	—	—
LAWSON LABORATORIES	134	4	16	12k	±5	—	—	—
	140	4	15	7.5	±5	—	—	—
METRABYTE	DASCON-1	4	12	30	±2.0475	—	1, 10, 100, 1000	SWITCH
	DASH-8	8 SE	12	4k	±5	—	—	—

*PROGRAMMABLE
**CARRIER BOARD AND MODULES

L = LABTECH NOTEBOOK
U = UNKELSCOPE
R = RTSS
C = CODAS
Q = QED
S = SNAPSHOT
A = ASYSTANT+
I = ILS
SE = SINGLE-ENDED
DI = DIFFERENTIAL

D/A CHANNELS	D/A RESOLUTION (BITS)	D/A RANGES (V)	DIGITAL I/O LINES	CLOCK/ COUNTERS	PRICE	VENDOR SOFTWARE SUPPORT	THIRD-PARTY SOFTWARE SUPPORT	COMMENTS
24 MAX	12	0 TO 5, ±5	72 MAX	PROGRAMMABLE COUNTER/ TIMER	$ 295	PC LAB SUBROUTINES, $249	—	CARRIER BOARD ACCEPTS ANALOG I/O ($425) AND DIGITAL I/O ($199) MODULES AND EXPANDER ($385) AND COVERSION ($425) PLUG-IN CARDS. SPECS DEPEND ON MODULES
—	—	—	—	PROGRAMMABLE 0.005-Hz TO 25-kHz CLOCK	$ 299	BASIC SUBROUTINES INCLUDED	—	HALF-SIZE A/D-CONVERTER CARD
8	12	0 TO 5, ±5, 4 TO 20 mA	—	—	$ 399	BASIC SUBROUTINES INCLUDED	—	HALF-SIZE D/A-CONVERTER CARD
2	12	0 TO 5, 0 TO 10, ±2.5, ±5, ±10	16	PROGRAMMABLE 130-kHz CLOCK	$1195 OR $1595	ATLAB SUBROUTINES, $449	—	SPECS DEPEND ON MODEL. DT2821-F IS FIXED AT EITHER 16 SE OR 8 DI A/D CHANNELS AT FACTORY
2	12	0 TO 5, 0 TO 10, ±2.5, ±5, ±10	16	PROGRAMMABLE 130-kHz CLOCK	$2495	ATLAB SUBROUTINES, $449	—	
2	12	0 TO 5, 0 TO 10, ±2.5, ±5, ±10	16	PROGRAMMABLE 130-kHz CLOCK	$1695	ATLAB SUBROUTINES, $449	—	SIMULTANEOUS S/H CAPABILITY
—	—	—	—	REAL-TIME CLOCK	$ 575	PREMAS, $175; CODAS, $895; I/O DRIVERS INCLUDED	—	PROGRAMMABLE A/D RESOLUTION TO 12, 16, OR 19 BITS
2	12	0 TO 5	4 STATUS	—	$1645	I/O DRIVERS INCLUDED; DASA SOFTWARE, $4000	L	SOFTWARE AVAILABLE IN SEPARATE MODULES
4	12	±10	32 MAX (OPTIONAL)	2 CHANNELS (OPTIONAL)	$1207	I/O DRIVERS INCLUDED	L	OPTIONAL DIGITAL I/O ($100) AND CLOCK/COUNTER ($225)
1	12	0 TO 1, 0 TO 2, 0 TO 5, 0 TO 10, ±0.5, ±1, ±2, ±5	24	4 TO 16 BITS, 10 Hz TO 250 kHz	$ 655	ADALAB INCLUDED	—	ADALAB-PC-DA ($985) INCLUDES ANOTHER D/A CHANNEL AND AN A/D CHANNEL; EXTN-PC OPTION ($402) PROVIDES 16 DI MUXED INPUTS
—	—	—	24 PER MODULE	3 16-BIT COUNTER-TIMERS PER MODULE	$ 220	DAISI/SOFT INCLUDED	L, U	CARRIER BOARD ACCEPTS A/D-CONVERTER ($450) AND DIGITAL I/O ($220) MODULES. SPECS DEPEND ON MODULE
—	—	—	4	—	$ 475	FASTSAMP INCLUDED; PC64, $150	—	
—	—	—	4	—	$ 265		—	
2 (OPTIONAL)	12	0 TO 5, 0 TO 10, ±2.5, ±5, ±10	12 BITS	REAL-TIME BATTERY BACKUP	$ 495	REAL-TIME GRAPHICS, SAMPLE PROGRAM INCLUDED	L	PROGRAMMABLE-GAIN AMPLIFIER ON 2 CHANNELS, RTD (RESISTANCE-TEMPERATURE DEVICE) INTERFACE ON REMAINING EXTERNAL INTERRUPTS FOR BACKGROUND OPERATION
—	—	—	3 INPUT, 4 OUTPUT	EVENT COUNTER, PULSE GENERATOR	$ 395	REAL-TIME GRAPHICS, SAMPLE PROGRAM INCLUDED	L, C, R	HALF-SIZE CARD

ANALOG I/O ADD-IN BOARDS FOR IBM PCs AND COMPATIBLES *(Continued)*

MANUFACTURER	BOARD	A/D CHANNELS	A/D RESOLUTION (BITS)	THROUGHPUT (SAMPLES/ SEC)	A/D RANGES (V)	A/D RANGE SELECTION	PROGRAM-MABLE GAIN	PROGRAM-MING METHOD
METRABYTE (Continued)	DASH-16	16 SE, 8 DI	12	50k	±5	—	0.5, 1, 2, 5, 10	DIP SWITCH
	DASH-16AF	16 SE, 8 DI	12	125k	±10	SWITCH-SELECT	0.5, 1, 2, 5, 10, OR RES SELECT	SWITCH-SELECT
	DAC-02	—	—	—	—	—	—	—
	DDA-06	—	—	—	—	—	—	—
MICROCOMPUTER SYSTEMS	PC MATE	4 SE	12	6k	0 TO 5, ±5, ±10	—	—	—
MICROSTAR LABORATORIES	DATA-ACQUISITION PROCESSOR	16 SE, 8 DI	14 (16 OPTIONAL)	17.5k	−10 TO +10, −5 TO +5	JUMPER	1, 2, 4, 8, 16, 32, 64, 128	SOFTWARE
MICROWAY	A2D-160	2	12	166k	0 TO 5, ±3, ±5	JUMPERS	—	SOFTWARE
QUA TECH	PXB-721** CARRIER BOARD	16 SE, 8 DI PER MODULE	8 OR 12	30k	0 TO 2.5, 0 TO 5, ±2.5, ±5; OR 0 TO 5, ±5	JUMPER	1, 10; OR 1, 10, 100	JUMPERS
SCIENTIFIC SOLUTIONS	LAB TENDER	32 SE, 16 DI	8	50k	±5	—	—	—
	DADIO	—	—	—	—	—	—	—
STRAWBERRY TREE	ACPC-16-8 ACPC-16-16	8 OR 16 DI	16*	200 OR 2500	−0.005 TO +0.005, −0.025 TO +0.025, −0.05 TO +0.5, −0.25 TO +0.25, −1 TO +10, −5 TO +5	SOFTWARE	1 TO 200	SOFTWARE
	ACPC-12-8	8 DI	12*	2.5k	−0.005 TO +0.005, −0.025 TO +0.025, −0.05 TO +0.5, −0.25 TO +0.25, −1 TO +10, −5 TO +5	SOFTWARE	1 TO 200	—
	ACPC-14-8-A	8 DI	14*	2.5	−0.005 TO +0.005, −0.025 TO +0.025, −0.05 TO +0.5, −0.25 TO +0.25, −1 TO +10, −5 TO +5	SOFTWARE	—	—
	ACPC-14-16-A	16 DI	14*	2.5	—	—	—	—
TAURUS COMPUTER PRODUCTS	KS101	16 SE, 8 DI	12	10k	0 TO 5, 0 TO 10, ±2.5, ±5, ±10	JUMPER	1 TO 1000	EXTERNAL RESISTOR
WITT ENGINEERING	PCA/88	1	8	66.7k	0 TO 5, 0 TO 10, ±5, ±10	JUMPER	—	—

*PROGRAMMABLE
**CARRIER BOARD AND MODULES

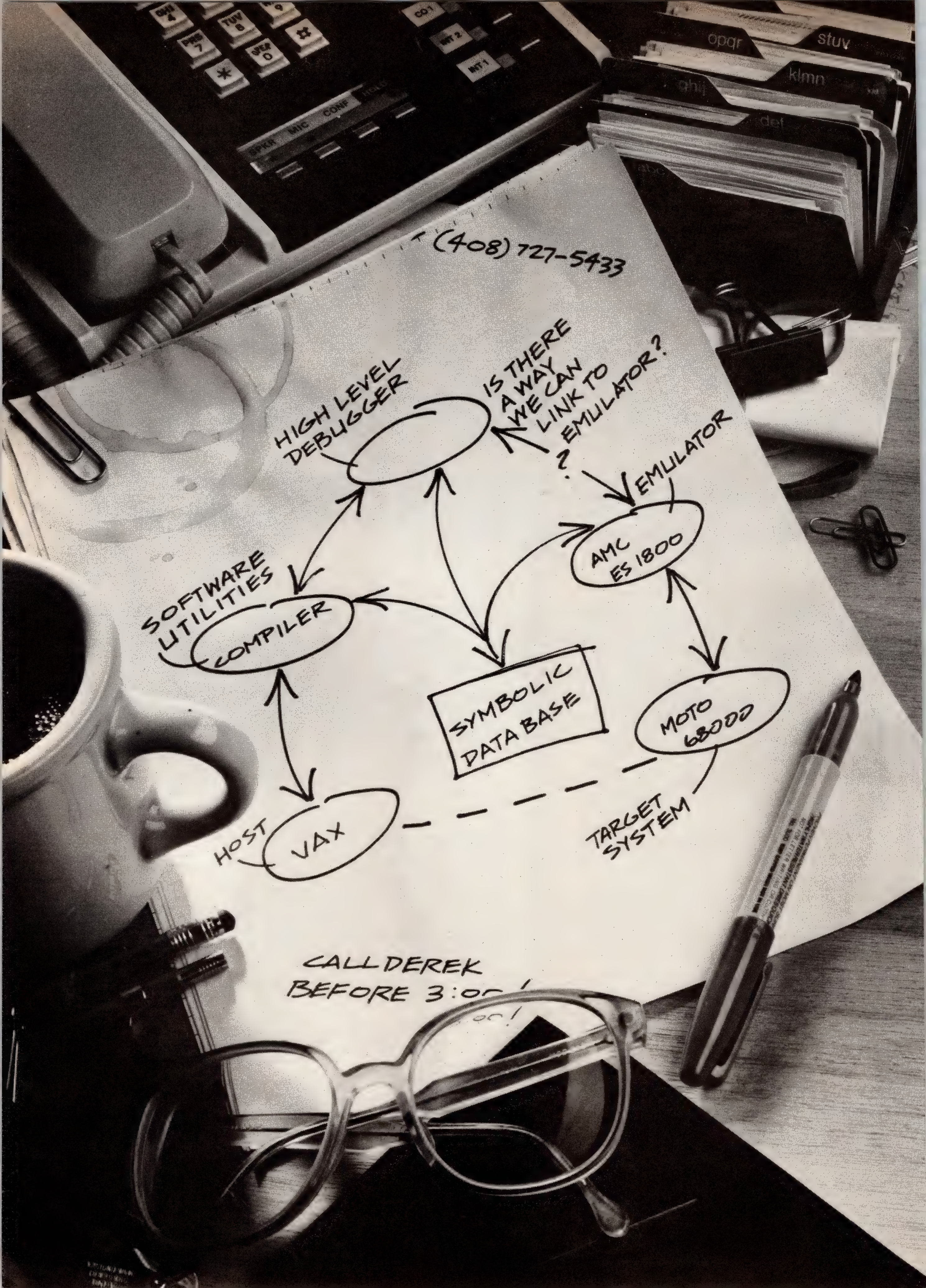
L = LABTECH NOTEBOOK
U = UNKELSCOPE

R = RTSS
C = CODAS

Q = QED
S = SNAPSHOT

D/A CHANNELS	D/A RESOLUTION (BITS)	D/A RANGES (V)	DIGITAL I/O LINES	CLOCK/ COUNTERS	PRICE	VENDOR SOFTWARE SUPPORT	THIRD-PARTY SOFTWARE SUPPORT	COMMENTS
2	12	0 TO 5	4 INPUT, 4 OUTPUT	EVENT COUNTER	$ 945	REAL-TIME GRAPHICS, SAMPLE PROGRAM INCLUDED	L, R, Q, U, S, A, C	
2	12	0 TO 5	4 INPUT, 4 OUTPUT	EVENT COUNTER	$1095	REAL-TIME GRAPHICS, SAMPLE PROGRAM INCLUDED	L, R, Q, U, S, A, C	BOARD INCLUDES MULTIPLYING D/A CONVERTER, ACCEPTS AC REFERENCE
2	12	0 TO 5, ±5, ±10, 4 TO 20 mA	12 BITS	—	$ 260	REAL-TIME GRAPHICS, SAMPLE PROGRAM INCLUDED	L	
6	12	0 TO 5, 0 TO 10, ±2.5, ±5, ±10, 4 TO 20 mA	3 8-BIT PORTS	—	$ 595	REAL-TIME GRAPHICS, SAMPLE PROGRAM INCLUDED	L	
4	8	0 TO 5, ±5, ±10	35	6 EVENT-COUNTER/ TIMERS	$ 995	I/O DRIVERS INCLUDED	—	2 SERIAL I/O PORTS
1	8	0 TO 10, ±10	3	PACER CLOCK	$2500	DAPL OPERATING SYSTEM	L	
1	9	±5	—	2	$1295	I/O DRIVERS INCLUDED	U	BOARD INCLUDES WHITE-NOISE GENERATOR; ANTI-ALIASING FILTERS ARE OPTIONAL ($225).
2 OR 8	8 OR 12	0 TO 5, ±5, ±2.5; OR 0 TO 5, ±5	72 ON CARRIER	CTM-10 MODULE	$ 195	LABSTAR INCLUDED	U	CARRIER BOARD REQUIRES FROM 1 TO 3 MODULES, WHICH COST $250 TO $595 EACH; SPECS DEPEND ON MODULES
16	8	±5	24	5 16-BIT COUNTERS, EVENT COUNTER, TIME-OF-DAY CLOCK	$ 495	I/O DRIVERS INCLUDED; LABPAC, $495	L, A, U	
4	12	0 TO 5, 0 TO 10, ±2.5, ±5, ±10	24	EXTERNAL TRIGGER	$ 395	LABPAC, $495	L, A	DOUBLE-BUFFERED D/A CONVERTERS CAN CHANGE SIMULTANEOUSLY
—	—	—	16	REAL-TIME CLOCK	$1290 OR $1590	MENU-DRIVEN PACKAGE AND SOURCE CODE INCLUDED	—	ACPC-16-8 OFFERS 2500-Hz PROGRAMMABLE RESOLUTION AT 12 BITS
—	—	—	16	—	$ 790	MENU-DRIVEN PACKAGE AND SOURCE CODE INCLUDED	—	
2	14	0 TO 10	16	—	$ 640	MENU-DRIVEN PACKAGE AND SOURCE CODE INCLUDED	—	
2	14	0 TO 10	16	REAL-TIME CLOCK	$ 840	MENU-DRIVEN PACKAGE AND SOURCE CODE INCLUDED	—	50-Hz PROGRAMMABLE RESOLUTION AT 8 BITS
2 (OPTIONAL)	12	0 TO 5, 0 TO 10, ±2.5, ±5, ±10	16	4 16-BIT, 8-MHz EVENT COUNTERS, (OPTIONAL)	$1360	T-SOFT101 INCLUDED	L	2 D/A CHANNELS AND EVENT COUNTERS, $380
1	8	0 TO 5, 0 TO 10, ±5, ±10	—	—	$ 169	I/O DRIVERS	—	

A = ASYSTANT+ SE = SINGLE-ENDED
I = ILS DI = DIFFERENTIAL



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HOSTS	OPERATING SYSTEMS	TARGETS	LANGUAGES	TOOLS
VAX	VMS	8048 family, 8080, 8085, 8086/88 and 80186/188	C	Assemblers
MicroVAX	ULTRIX	6800/2/8, 6809/9E, 68000/8/10 and 68020	Pascal	Linkers
UNIX-oriented workstations · Apollo · Sun · IBM AT	UNIX	Z80, MK3880/4 and Z8001/2/3	FORTRAN	Locaters
MS-DOS workstations · PC · PC XT · PC AT	XENIX	NSC-800	PL/M	Compilers
	MS-DOS		Assembler	Symbolic debuggers
				Source-level debuggers

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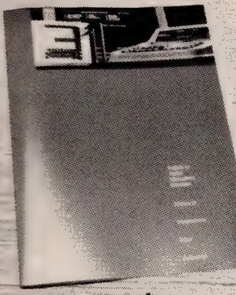
Validate™ links emulation with symbolic and source-level debugging.



When your software engineers only speak C and your emulator only speaks assembler, your development tools are worse than worthless. If your function is in assembler and your debugger speaks only C, you've got the same problem. The power of the Validate environment is that it works equally in high level languages and in assembler. You don't sacrifice any power or any comfort.

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CIRCLE NO 100

NCC '86

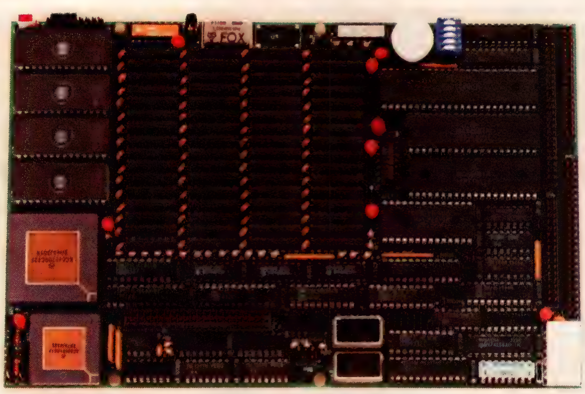
The sessions planned for NCC '86 reflect the show's recent shift towards presenting topics for computer end-users. However, you'll be able to take advantage of the show's liberal sprinkling of sessions on artificial intelligence, CAE, communications, and hardware, and you can visit more than 600 product displays.

Maury Wright, *Regional Editor*

Continuing its trend toward providing information for computer end-users, the 1986 National Computer Conference (NCC) will focus primarily on topics in data processing and management information systems (MIS). And because the computer end-user is typically concerned more with software than with hardware, the conference sessions strongly emphasize software rather than hardware topics. Nevertheless, NCC offers for the design engineer ample coverage of artificial-intelligence (AI), CAE, data-communication, and hardware topics. Moreover, you'll be able to view products ranging from ICs through supercomputers at the exibition accompanying the sessions.

The 4-day conference, which will take place June 16 through 19 in Las Vegas, NV (see **box**, "NCC '86 registration details"), will offer more than 100 sessions in 15 program tracks. The conference sessions will cover a variety of general computer topics such as AI, networking, management issues, end-user computing, educational and societal issues, software, hardware, and case studies.

The track on networking will include a session on local-area networks. The session, which will target a technical audience, will focus on a number of LAN vendors and products. Participants will discuss basic design concepts and actual vendor implementations.



***Among the products you can see at NCC '86** is the Micro-20 CPU board from GMX. Featuring 2M bytes of RAM and a 256k-byte EPROM, the board hosts either a 12.5- or a 16.67-MHz µP. It includes peripheral controllers and I/O ports; a 68881 processor is optional.*

Another session in the networking track will concern networking software. The session will examine the inability of multiple networks to communicate. Participants will discuss the solution that networking software offers for this incompatibility problem. Other discussions of networking are scheduled for a session on network management and one on international networking.

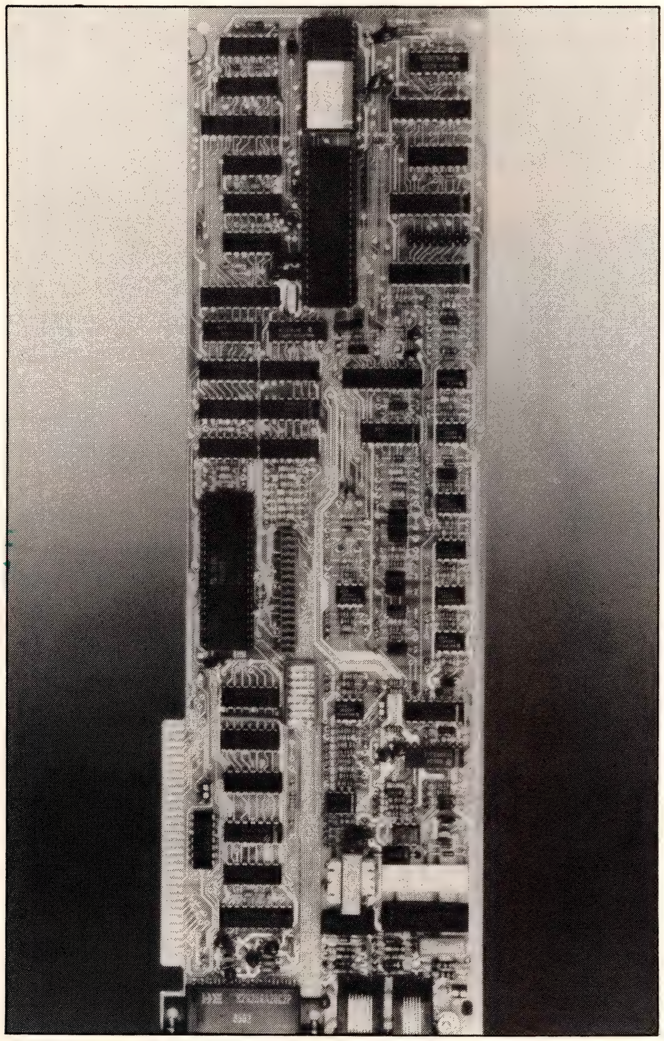
You'll also find a track of sessions on artificial intelligence. The session entitled "The marriage of expert systems and simulation," for instance, will discuss the application of knowledge-based program techniques in computer-based simulation. Speakers will consider the contribution of AI to simulation; topics covered will range from program development to the analysis of simulated results. Another session in the AI track will cover current applications of AI microcomputers to CAD and CAM.

A couple of the AI sessions will explore the tradeoffs involved in using various hardware platforms for AI. For instance, the session entitled "Expert systems:

Mainframe or microcomputer?" will explore the use of expert systems in mainframe, minicomputer, and microcomputer environments and touch on new uses for, and real-time applications of, these systems. Panelists will debate whether expert systems can be used effectively with microcomputers.

Because the conference emphasizes software, it's not surprising that some of the topics in the software track overlap with topics covered in other tracks. For example, the session entitled "Can software help software development? The case for expert systems" will explore intelligent support for software development.

Despite this concentration on software, however, the conference's hardware and engineering tracks will offer some discussions of hardware design. Sessions on hardware will focus primarily on box-level equipment such as printers.

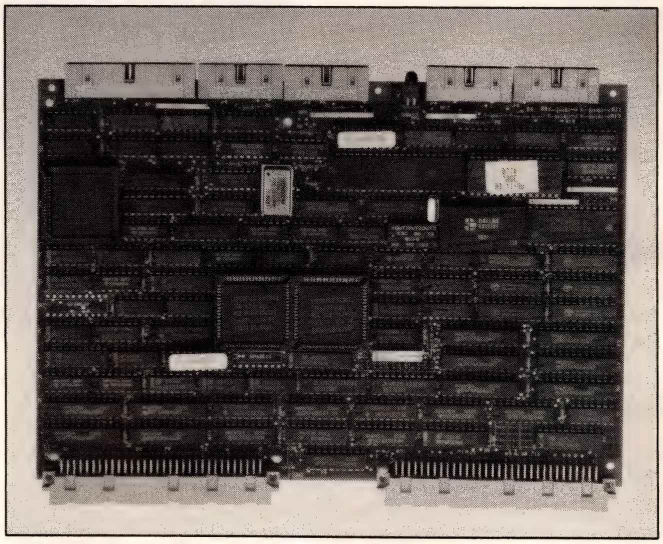


Providing compatibility with IBM mainframes, *the $895 Sync-up 201C modem card for the IBM PC comes with IBM-compatible BiSync software. The card, from Universal Data Systems, provides 2400-baud communications.*

The hardware session entitled "Semiconductor directions in connectivity," will cover trends in VLSI that promise to meet connectivity needs in the office for network and graphics applications. Scheduled for the same time slot is the session entitled "Will new architecture save the minicomputer industry?" The discussion will focus on fault-tolerant and RISC architectures.

The hardware track will also include a consideration of contemporary applications of speech technology (voice I/O) in office automation, factory automation, and defense. Another session, "Smart facilities in support of smart systems," will focus on the design and cost of building infrastructures in support of advanced networks and information systems. Other hardware sessions will investigate emerging storage technologies and architectures, the implications of optical storage technology in the automated office, and customer-service issues.

In the engineering track, the sessions will focus mainly on CAD, CAE, and CAM topics. The session called "Graphics/workstation technology trends," for example, will examine price and performance trends in workstations and probe the workstations' graphics functions. Another session will discuss the future of



This VME/ESDI disk controller, *Model 712 from Xylogics, supports the 32-bit VME Bus interface.*

CAD/CAM productivity and offer ways for manufacturers to use the technology to significantly improve their productivity.

In addition to conference sessions, NCC will offer professional-development seminars. These half-day or full-day seminars will provide self-improvement and management training. Among the seminars offered will be a roundtable discussion on supercomputers, an examination of computer crime, an AI workshop, a talk on software development under Unix, and a course on improving your business and professional writing skills. Some of the seminars will give you the opportunity to get hands-on experience with AI, networking, and Unix. Further, two seminars will teach advanced techniques for using the Lotus 1-2-3 and dBaseIII spreadsheet programs.

Thursday's sessions will be open to all registrants of the NCC exhibition, whether or not they've registered for the conference sessions. The two tracks will highlight research and development in the computer industry and small businesses. The track on R&D will consist of 14 30-minute presentations, each followed by 10-minute question-and-answer sessions. The presentations will mainly cover software topics. Speakers will probe such issues as source-file management under Unix, detecting loop structure in assembly code, nonchronological sequential simulation, applying software reliability models to decision support, and privacy in digital communications.

These 300-dot/in. image scanners, *the MS-300 family from Microtek Lab, can perform character recognition when used with third-party software in a personal-computer-based environment.*

The track on small businesses will consist of four 1½-hour consecutive sessions. The sessions will provide a forum for executives and owners of small businesses having sales volumes between $1 million and $50 million. The sessions offer participants the opportunity to learn about the purchasing process and application of small business computers.

Product exhibition

At the exhibition accompanying the NCC '86 professional program, you'll be able to view more than 600 product displays. Vendors will show a variety of products—such as ICs, board-level computers, graphics and

NCC '86 registration and schedule details

The National Computer Conference for 1986 will take place Monday, June 15, through Thursday, June 19, at the Las Vegas Convention Center and Las Vegas Hilton Hotel. Consult the **schedules** appearing on pg 148 through 154 for the dates and times of the conference sessions, complimentary program, and seminars.

Advance registration fees for the conference program are $100 for one day, $200 for the entire conference. Registration at the door costs $250; you can register on Sunday from 1 to 5 PM, Monday through Wednesday from 8 AM to 6 PM, and Thursday from 8 AM to 4 PM at the Las Vegas Convention Center. The professional-development seminars cost $125 for a half day and $200 for a full day; registrants can earn continuing-education units by participating in these seminars.

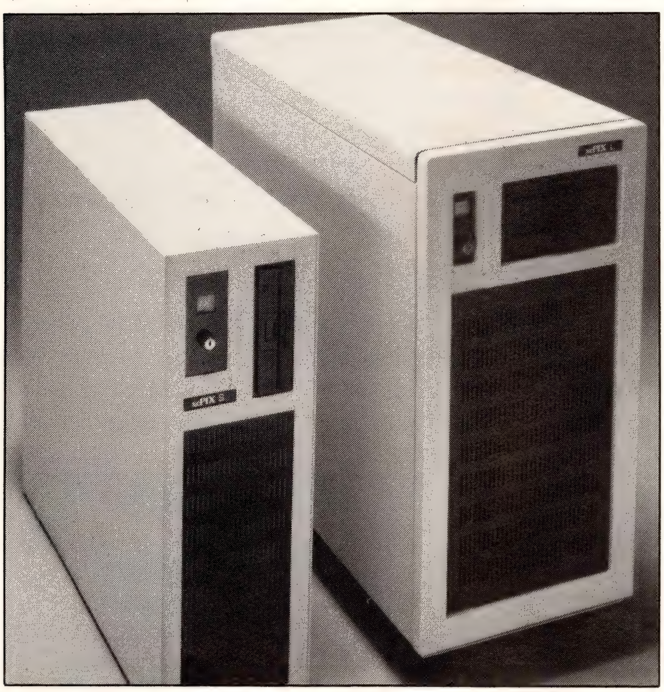
Special events at NCC will include the keynote address, which will be delivered by Robert L Crandall, chairman of AMR Corp (the parent company of American Airlines) on Monday, June 15, from 9:30 to 11:30 AM in the Las Vegas Hilton's ballroom. Crandall was the driving force behind the development of American Airline's Sabre automation system for travel agents.

People who register for the exhibition only ($25 in advance) may also attend the complimentary sessions on Thursday, as well as exhibitor forums. Tickets to the forums will be available at the exhibitors' booths. Finally, all registrants are invited to attend the NCC '86 kickoff reception on Sunday, June 15, from 2 to 6 PM at Caesar's Palace, Las Vegas, NV.

To register, obtain further information, or request conference proceedings, write to The 1986 National Computer Conference, 1899 Preston White Dr, Reston, VA 22091, or call (800) 622-1986; in VA, (703) 620-8955.

communications devices, and supercomputers—in the exhibit hall from 10 AM to 6 PM Monday through Wednesday and from 10 AM through 4 PM Thursday.

Among the ICs on display at NCC will be Motorola's MC10320, a triple video D/A converter. The IC, which the company will introduce at the exhibition, includes three 4-bit DACs and a 16×12 color-look-up-table RAM on a 28-pin monolithic IC. The IC supports a 150-MHz pixel rate and includes an internal reference, as well as sync and blank inputs. The IC, which costs $42 (1000), accepts user-selectable TTL or ECL inputs and provides RS-343-A-compatible outputs.



Providing 3-MIPS performance, *the Gator Series 68020-based supermicrocomputers from Xepix sell for as little as $5000 in OEM quantities.*

You'll also have the opportunity to examine a number of board-level products. Xylogics, for instance, will exhibit its Model 712 VME/ESDI disk controller. The controller, which sells for $1295 (1000), supports the full 32-bit VME bus interface.

GMX will introduce a 68020-based single-board computer. The CPU board, Model Micro-20, hosts either a 12.5- or a 16.67-MHz μP. A 68881 floating-point coprocessor is optional. The board's memory capabilities include 2M bytes of RAM and a 256k-byte EPROM. The board also includes four serial ports, a parallel port, a floppy-disk-drive interface, an SASI interface, and a battery-backed clock. A 12.5-MHz Micro-20 costs $2750.

You can also expect to find some graphics devices at NCC. For example, Video Monitors will exhibit its M2400 family of monochrome monitors, which offer horizontal scan frequencies ranging from 15.75 to 85 kHz and vertical refresh frequencies ranging from 45 to 120 Hz. The monitors are available with analog-, TTL-, and ECL-input options, and their CRT sizes range from 7 to 23 in. A typical 20-in. model with a standard chassis and a switching power supply costs $535 (1000).

Hard-copy graphics devices on display will include the Houston Instrument DMP-56 pen plotter. The plotter accepts 18 different media sizes, including A- to E-size drawings. It employs the DM/PL firmware command language and interfaces to a host via an RS-232C port. The $5995 plotter features 0.001-in. resolution and 17-in./sec velocity.

Image scanners or digitizers will also figure prominently among the graphics exhibits. Microtek Lab will exhibit the MS-300 family of document scanners, which

For more information . . .

For more information on the NCC '86 products discussed in this article, contact the following manufacturers directly or circle the appropriate numbers on the information Retrieval Service card.

GMX Inc
1337 W 37th Pl
Chicago, IL 60609
(312) 927-5510
Circle No 691

Houston Instrument
8500 Cameron Rd
Austin, TX 78753
(512) 835-0900
Circle No 692

Microtek Lab Inc
16901 S Western Ave
Gardena, CA 90247
(213) 321-2121
Circle No 693

Motorola Inc
Box 2953
Phoenix, AZ 85062
(602) 244-6900
Circle No 694

Universal Data Systems
5000 Bradford Dr
Huntsville, AL 35805
(205) 837-8100
Circle No 695

Video Monitors Inc
3833 N White Ave
Eau Claire, WI 54703
(715) 834-7785
Circle No 696

Xepix Inc
51 Lake St
Nashua, NH 03060
(603) 881-8791
Circle No 697

Xylogics Inc
144 Middlesex Tpk
Burlington, MA 01803
(617) 272-8140
Circle No 698

Take a good long look at your performance and system integration needs. Now take a look at two Microbar Multibus™-based boards for the 68020—Multibus I and Multibus II.

Needless to say, we look very, very good.

Witness, for example, 32-bit performance on a single board. And you can have it *now*. Not next year or down the road, but right now (after all, we do understand the window of opportunity you're up against).

Nice enough, but there's more.

Like the 68020 with MMU, DMA and Floating Point capabilities. RAM, from 1MB to more than 4MB—all high-speed with dual-ported access. Two serial ports and a parallel port. We also provide UNIX™ System V and real-time operating systems ported to the CPU.

However, while the above is all great and wonderful, it is by no means the whole story.

Our boards deliver ideal performance of the microprocessor as well as thorough integration with the standard system bus architecture.

You'll also grow quite fond of the software portability, allowing existing 68000 software to be executed by the 68020—while more than doubling performance.

And lest we forget, the on-board architecture of our GPC68020 for Multibus I is compatible with your next-generation system's evolutionary path using our Multibus II MT68020 board.

So, when your team wants to go to town, call us in California at (800) 421-1752 or (800) 821-1011 within the Continental U.S.

We'll give you the Microbar muscle to move in quantum leaps.

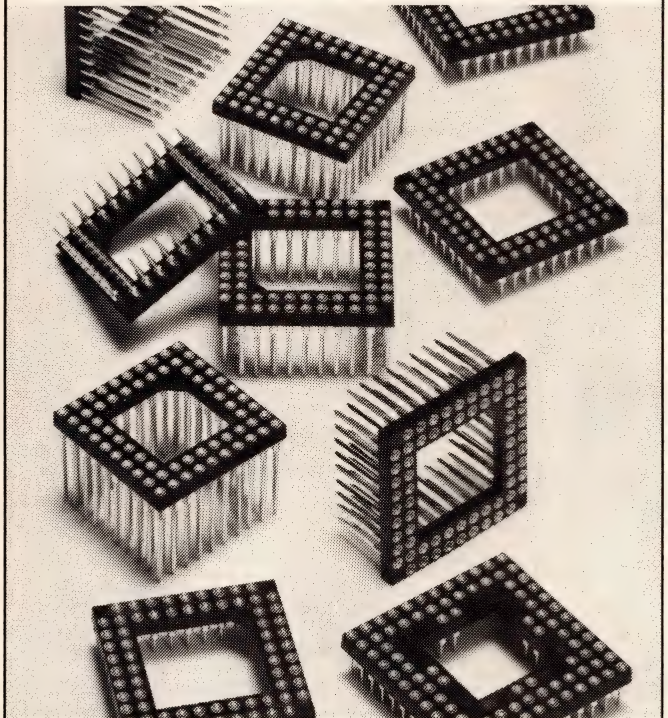
68020 Multibus Boards. Ready and waiting for design teams taking quantum leaps.

MICROBAR SYSTEMS, INC.
785 Lucerne Drive, Sunnyvale, CA 94086
Your future system is our current project.

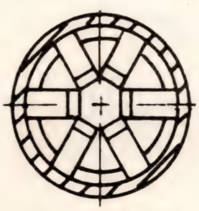
™ UNIX is a trademark of AT&T.
™ Multibus is a trademark of Intel Corp.

CIRCLE NO 101

2½ oz
Average Insertion Force



Lowest insertion and extraction force P.G.A. sockets available . . . only 2½ oz. average insertion force per pin.



Cross Section of new 6 finger socket.

- New 6-finger beryllium copper contacts offer 6 points of reliable contact.
- Over 150 P.G.A. footprints, 12 to 324 pins...custom designs delivered in 2 to 3 weeks.
- Most sockets available with molded bodies.
- Terminals available in Standard Low, Super-Low and Ultra-Low profiles and Wire-Wrap®.
- Insulators in molded polyester, .062 glass epoxy, or Peel-A-Way™ in Mylar® or Kapton®.

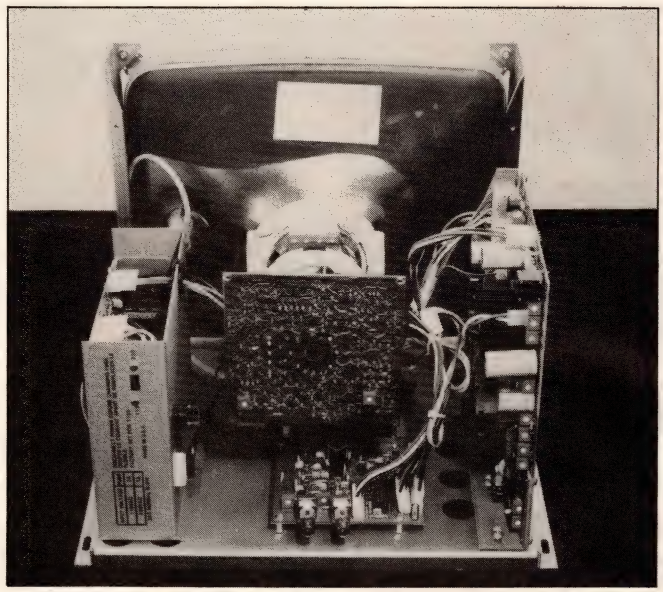
Wire-Wrap — ® Gardner-Denver
Mylar & Kapton — ® Dupont Chemical

Call or write for more information.

US Patent #4442938 and Patents Pending

ADVANCED INTERCONNECTIONS
5 Division Street, Warwick, RI 02818 • (401) 885-0485
TWX 710 3820400

CIRCLE NO 102



Available with 15.75- to 85-kHz horizontal scan frequencies, *the M2400 family of monochrome monitors from Video Monitors offers CRTs that range from 7 to 23 in.*

offer a resolution of 300 dots/in. The scanners cost around $2500; with third-party software, they're able to recognize characters for word processing.

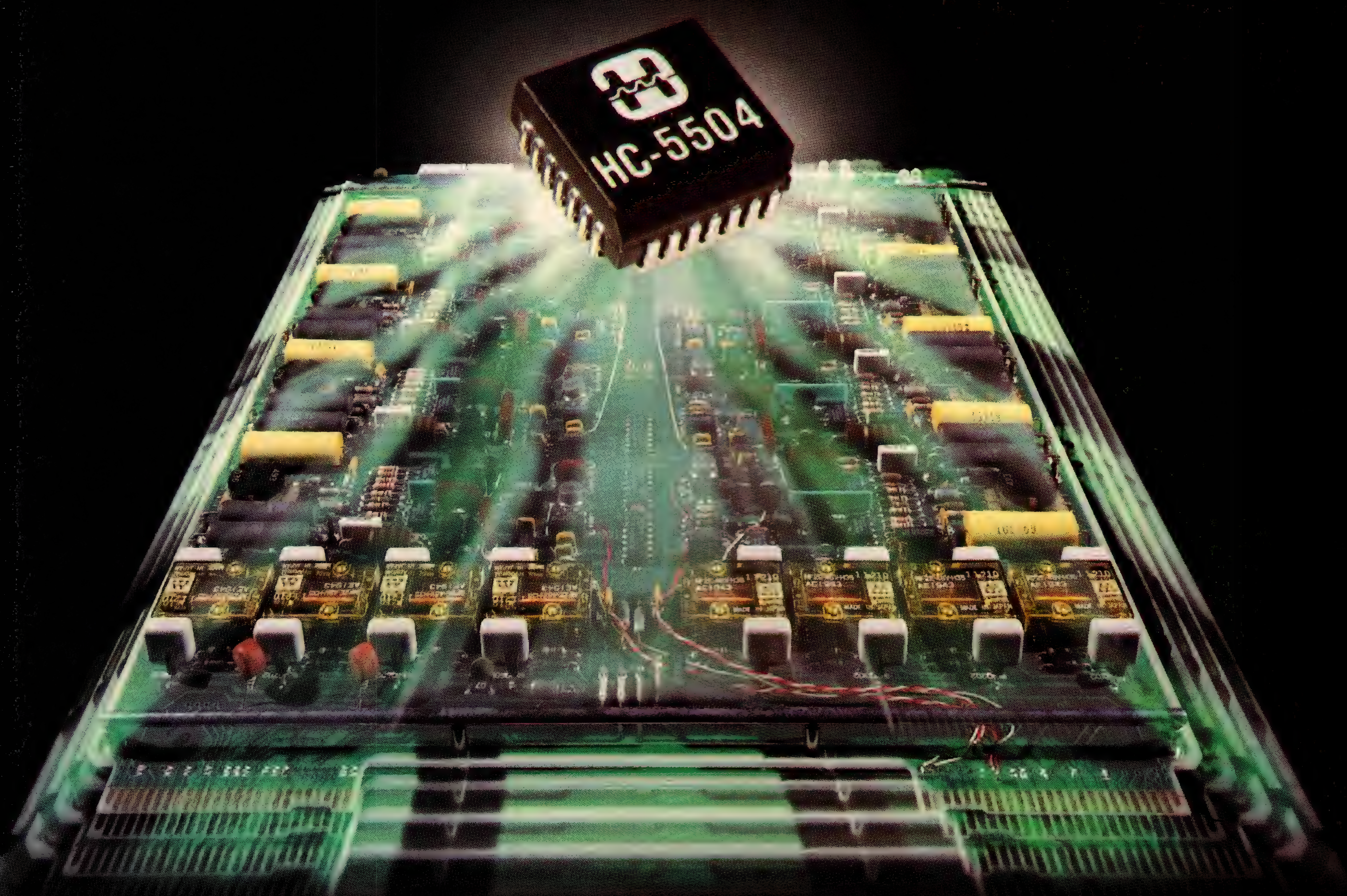
Exhibitors will also present a number of communications devices, including modems, multiplexers, and protocol converters. Universal Data Systems, for instance, will exhibit five new communications products, including the Sync-up 201C modem card for the IBM PC. The modem card provides 2400-baud communications and costs $685 with standard synchronous communications software. With IBM-compatible BiSync software, it costs $895. The company will also display the Sync-up 208A/B modem card, which costs from $1200 to $1410 and provides 4800-baud operation on private lines.

Finally, NCC '86 will feature a number of the new supercomputers in microcomputer, minicomputer, and mainframe hardware platforms. For example, you'll have the opportunity to examine the Gator Series 32-bit Unix systems from Xepix. The 68020-based systems provide 3-MIPS performance. Including CPU, memory, I/O, and mass-storage capability, the systems cost from $5000 to $10,000 in OEM quantities. **EDN**

Article Interest Quotient (Circle One)
High 473 Medium 474 Low 475

Schedules begin on pg 148

Shrink Your Board Size with Harris Telecom ICs.



LICs, CODECs, Filters, Combos, CVSDs, T-1, ISDN... Harris Semiconductor offers telecom designers a broad-based line of top-quality integrated circuits, supporting an almost endless roster of communications applications. A comprehensive line of ICs gives you the Harris competitive edge throughout the subscriber loop and telephone network. In addition, Harris offers an impressive array of dedicated, high-performance, low-power CMOS data communications ICs. For details on these and other exciting products, write: Harris/MHS Semiconductor Sales Ltd., Eskdale Road, Winnersh, Wokingham, Berks, RG11 5TR, England.

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CIRCLE NO 103

NCC '86 CONFERENCE SESSIONS

PROGRAM TRACK	MONDAY JUNE 16 9:30-11:00 AM	MONDAY JUNE 16 1:30-3:00 PM	MONDAY JUNE 16 3:30-5:00 PM	TUESDAY 8:30-10:00 AM	TUESDAY 10:30 AM-12:00 PM
ARTIFICIAL INTELLIGENCE	KEYNOTE ADDRESS *ROBERT L CRANDALL, CHAIRMAN, AMR CORP*	CONTRIBUTIONS OF AI TO EDUCATION *WAYNE HARVEY, STANFORD RESEARCH INSTITUTE*	THE MARRIAGE OF EXPERT SYSTEMS AND SIMULATION *NORMAN NIELSEN, STANFORD RESEARCH INSTITUTE*	EXPERT SYSTEMS: MAINFRAME OR MICROCOMPUTER? *ROBERT ANDERSON, THE RAND CORP*	AN AI APPROACH TO DOCUMENT PREPARATION *MARTHA EVENS, ILLINOIS INSTITUTE OF TECHNOLOGY*
NETWORKING		INTEGRATED SERVICES DIGITAL NETWORKS *PHILIP BEIDELMAN, WESTERN TELE-COMMUNICATIONS CONSULTING* LOCAL-AREA NETWORKS *J EDWARD SNYDER, TRW INFORMATION NETWORKS DIV*	TELECOMMUNI-CATIONS IN THE INFORMATION AGE *RICHARD LEIBHABER, MCI*	INTERNATIONAL NETWORKING *WILLIAM BRASUELL, TANDEM COMPUTERS*	A MANAGEMENT OVERVIEW *JOSEPH CLARK, JOSEPH CLARK AND CO*
MANAGEMENT ISSUES			ROLE OF THE INFORMATION-SYSTEMS MANAGER AS A CHANGE AGENT *ALLEN SMITH, ATLANTIC RICHFIELD*	CHANGE IS ROUTINE FOR INFORMATION SYSTEMS *KATHY BRITTAIN WHITE, UNIVERSITY OF NORTH CAROLINA*	INVENTING THE FUTURE—COMPETI-TIVE ADVANTAGE *VICTOR JANULAITIS, POSITIVE SUPPORT REVIEW*
END-USER COMPUTING		JUSTIFYING INVESTMENTS IN END-USER COMPUTING *N DEAN MEYER, DEAN MEYER & ASSOCIATES*	THE 4-4-4 CHALLENGE: IMPLICATIONS OF SUPERWORK-STATIONS FOR INFORMATION-SYSTEMS MANAGEMENT *BRIAN BLACKMARR, BRIAN BLACKMARR AND ASSOCIATES*	CHANGING CAREER PATHS FOR IS PROFESSIONALS AND MANAGERS *KATHY RICHARDS, FIREMEN'S FUND*	VENDOR SERVICE AND SUPPORT—WHAT'S IMPORTANT? *ALEXIA MARTIN, SEYBOLD OFFICE COMPUTING GROUP*
EDUCATIONAL AND SOCIETAL ISSUES		ERGONOMICS AND THE AUTOMATED OFFICE *ROBERT WILSON, HAMILTON-SORTER*			EDUCATIONAL TELE-COMMUNICATIONS *JUDITH JOHNS HUBNER, NATIONAL COMMIS-SION ON INDUSTRIAL INNOVATION*
SOFTWARE		FROM PROGRAM-MING TO SOFTWARE ENGINEERING *LES BELADY MCC*	MODELS, METHODS AND TOOLS FOR SOFTWARE DEVELOPMENT *CV RAMAMOORTHY, UNIVERSITY OF CALIFORNIA AT BERKELEY*	DO WE HAVE PACEMAKERS IN SOFTWARE? COBOL? UNIX? ADA? *JEAN SAMMET, IBM*	FOURTH-GENERATION LANGUAGES AND APPLICATION GENERATORS *WINSOR BROWN, DOUGLAS AIRCRAFT CO*
HARDWARE		MULTIVENDOR ENVIRONMENT—THE USER'S PERSPECTIVE *RICHARD PRICE, PEABODY HOLDING CO*	SERVICE ISSUES *PAUL VILANDRE, CONVERGENT TECHNOLOGY CORP* NEW DIRECTION IN PRINTER TECHNOLOGY—THE THE AGE OF ELEC-TRONIC IMAGING *CHARLES PESKO, PESKO ASSOCIATES*	CONTEMPORARY APPLICATIONS OF SPEECH TECHNOLOGY *STANLEY GOLDSTEIN, MEDIA DIMENSIONS* UNDERSTANDING PARALLELISM AND ITS USE IN SUPERCOMPUTERS *PAUL SCHNECK, SUPER COMPUTING RESEARCH CENTER*	DEPARTMENTAL COMPUTING: PANACEA OR SOLUTION? *GEORGE COLONY, FORRESTER RESEARCH* IMPACT AND IMPLICATIONS OF OPTICAL STORAGE TECHNOLOGY WITHIN THE AUTOMATED OFFICE *JOHN WALSH, INTEGRATED STRATEGIES*

	JUNE 17		WEDNESDAY JUNE 18			
	1:30-3:00 PM	3:30-5:00 PM	8:30-10:00 AM	10:30 AM-12:00 PM	1:30-3:00 PM	3:30-5:00 PM
		AI MICROCOMPUTER APPLICATIONS IN CAD/CAM *WILLIAM SALMON, SALTEK SERVICES*	UNCERTAINTY IN INTELLIGENT SYSTEMS *RONALD YAEGER, IONA COLLEGE*		PROGRAMMING LANGUAGES FOR ARTIFICIAL INTELLIGENCE *SHELDON BORKIN, IBM, CAMBRIDGE SCIENTIFIC CENTER*	
	NETWORK MANAGEMENT *ROBERT LINEBARGER, BRIGHAM YOUNG UNIVERSITY* CABLING SYSTEMS AND MICRO/-MAINFRAME COMMUNICATIONS *SIDNEY HARRIS, GEORGIA STATE UNIVERSITY*	CASE STUDIES *GORDON LEW, AMERICAN AIRLINES*	CONFERENCING *THOMAS HOUSAL, UNIVERSITY OF SOUTHERN CALIFORNIA*	ELECTRONIC MAIL *RICHARD GUNTHER, McDONNELL-DOUGLAS INFORMATION SYSTEMS GROUP*	LONG-DISTANCE ALTERNATIVES *GWYNDA MYERS, THE JIA GROUP*	NETWORKING SOFTWARE *CHRIS HUGHES, INTEL*
	WHO REALLY IS THE BOSS *PAUL DALI, REGIS McKENNA*		FINALLY, SHOES FOR THE COBBLERS' CHILDREN *RICHARD CARPENTER, INTECH*		HOW WASHINGTON REGULATES THE INFORMATION AGE *HOWARD FUNK, IBM*	
	WHAT MIS MANAGERS DON'T UNDERSTAND ABOUT THE OFFICE *LINDA O'KEEFE, DATAQUEST*	PERSONAL COMPUTERS TO OFFICE AUTO-MATION: BUILDING A SYSTEM *AMY WOHL, WOHL ASSOCIATES*	MANAGING THE TRAINING FUNCTION *CHARLES HOERNER, INFORMATION TECHNOLOGY CONSULTING*	OPTICAL DISKS AND LARGE DOCUMENT IMAGE SYSTEMS *MIKE ALSUP, ARTHUR ANDERSEN & CO*	FUTURE TRENDS IN END-USER INTERFACE *JIM BAIR, HEWLETT-PACKARD*	END-USER ACCESS: TRANSACTIONS AND INFORMATION *ANDREW FINN, AT&T* NEWS FROM RESEARCH PRO-GRAMS IN END-USER COMPUTING *TORA BIKSON, THE RAND CORP*
				ADMINISTRATIVE AND INSTRUCTIONAL USE OF COMPUTERS IN EDUCATION *HERBERT WITT, OFFICE OF INSPECTOR GENERAL*		HOW GOES THE COMPUTER REVOLUTION *NORMAN LIVERGOOD, UNIVERSITY OF SAN FRANCISCO*
	CAN SOFTWARE HELP SOFTWARE DEVELOPMENT? THE CASE FOR EXPERT SYSTEMS *BARBARA BRAWN, IBM* LET'S TALK ABOUT FRIENDLINESS, USABILITY, ICONICITY, WINDOWING	MANAGING THE SOFTWARE DEVELOPMENT PROCESS *PETER FREEMAN, UNIVERSITY OF CALIFORNIA AT IRVINE*	VIEWS AND PERSPECTIVES OF THE FUTURE OF DATABASES AND GRAPHICS *GERALD MARRONE, CITICORP*	SOFTWARE MAINTENANCE—OBSERVING THE PROFESSIONALS *NICHOLAS ZVEGINTZOV, SOFTWARE MAINTENANCE NEWS* SOFTWARE METRICS; HOW HOW DOES YOUR SOFTWARE SCORE?	IS THERE SUCH A THING AS PROGRAMMERS' PRODUCTIVITY?	SOFTWARE TESTING: THE BUG BUSTERS GROW UP! *E F MILLER, SOFTWARE RESEARCH INC* CAN YOU ACTUALLY MANUFACTURE SOFTWARE? HOW?
	SMART FACILITIES IN SUPPORT OF SMART SYSTEMS *MICHAEL BELL, HARBINGER GROUP*	WILL NEW ARCHI-TECTURE SAVE THE MINICOMPUTER INDUSTRY? *WILLIAM ROSSER, GARTNER GROUP* SEMICONDUCTOR DIRECTIONS IN CONNECTIVITY *BOBBIE FOX, INTEL*	EMERGING STORAGE TECHNOLOGIES AND ARCHITECTURES—JUDGING REAL AVAILABILITY FOR FUTURE SYSTEMS *JAMES MOORE DATAQUEST*	ARE YOU KEEPING PACE WITH THE FUTURE? *PAUL DALI, REGIS McKENNA*	IS THERE A SHAKEOUT COMING IN IBM OPERATING SYSTEMS? *MICHAEL BRAUDE, GARTNER GROUP*	

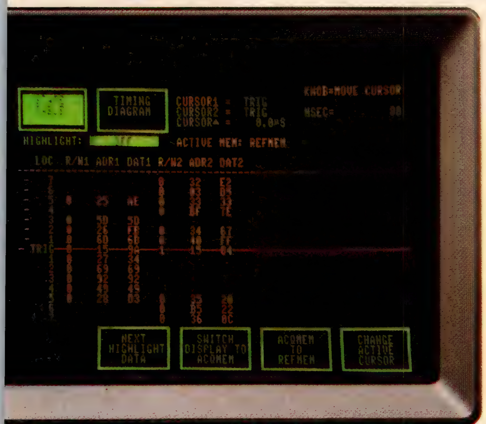
Continued on pg 152

TEK'S NEW COLOR LOGIC ANALYZER: MORE ACCURACY FOR MORE PRODUCTIVITY.

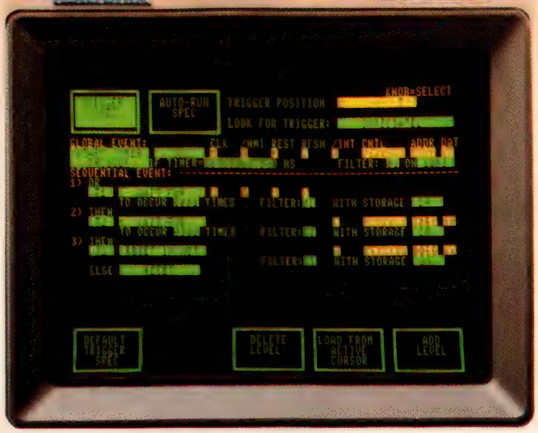
Meet the new 1241—one more reason why Tek's versatile 1200 Series offers you the best of the leading logic analyzers:

1 The 1241's color interface quickly guides your eye to the most relevant information. Analysis is faster. Easier on the eyes. You are more accurate, more productive. For extra readability, a vertical expansion feature doubles the height of the timing diagrams.

2 Like all members of the 1200 Series, the 1241 clearly



shows what your hardware and software are doing at the same time. For integrating partitioned designs, only the 1200 Series' Dual Timebase feature accurately depicts real-time interactions between independently-clocked modules. This lets you monitor relationships between two processors, or between hardware and software. Combine Dual Timebase with performance analysis on the 1241 to analyze the entire system and software performance. Monitor,



for example, the range of time spent by one processor waiting for a service request response from a second processor. The 1241's histogram display and 10ns resolution make these measurements clear and precise.

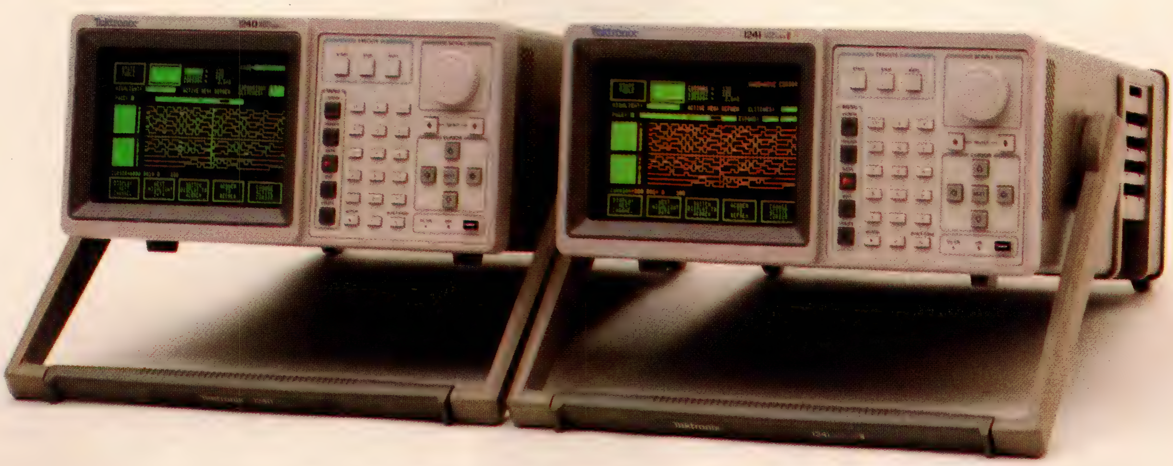
3 For both hardware and software analysis, Tek offers unsurpassed triggering. Software problems are pinpointed by 14 levels of conditional triggering combined with data and program flow qualification. Triggering on the timing characteristics, as well as the state of the hardware activity, is made possible by counters, timers, and duration filters.

4 Ease of use extends beyond the color screen. Four distinct levels of operation add features as your design challenges require. A unique touch-screen menu display lets you select over 50 high-level commands right off the screen. The big front panel knob provides flicker-free scrolling.

5 Modular, expandable and versatile, Tek's 1200 Series keeps costs low and compromises few. Support for all major microprocessors includes three types of disassembly. With 14 combinations of 9- or 18-channel acquisition cards, you configure the best data width (up to 72 channels), memory depth (up to 2K) and sample rate (up to 100 MHz). Add ROM packs for data analysis; RAM packs for storage; COMM packs for RS-232 and GPIB links to computers, plus printer interfacing; and master/slave capability

that links two systems via modem for teleservicing.

The 1241 is the newest reason why Tek is the logic analyzer leader. For more information or a demo, call 1-800-245-2036. In Oregon, call 231-1220. Or contact your local Tek Sales Engineer.



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Circle 104 for Literature

Circle 143 for Sales Contact

NCC '86 CONFERENCE SESSIONS

PROGRAM TRACK	MONDAY JUNE 16			TUESDAY	
	9:30-11:00 AM	1:30-3:00 PM	3:30-5:00 PM	8:30-10:00 AM	10:30 AM-12:00 PM
TRENDS			COMPUTER-SUPPORTED DECISION MAKING IN THE REAL-ESTATE INDUSTRY *MARK SWENSON, HOMART DEVELOPMENT CO*		
CASE STUDIES		BUILDING A $350,000,000 COMPUTER COMPANY *JOHN SINGLETON, PACIFIC AUTOMATION CO*	ISSUES WITH LARGE-SCALE IMPLEMENTATIONS *MIKE HESCHEL, AMERICAN HOSPITAL SUPPLY CORP*	ELECTRONIC PUBLISHING WITH OR WITHOUT PAPER *CONSTANCE GREASER, THE RAND CORP*	
CONTROVERSY		CAN SOFTWARE EVER MEET LEGISLATED WARRANTIES? *ED BRIDE, SOFTWARE NEWS*		ARE USER APPLICATIONS PROGRAMMERS BECOMING OBSOLETE? *TOM RUSH, COOPERS & LYBRAND*	DO CURRENT SOFTWARE PROTECTION AND PRICING PRACTICES CONSTITUTE A RAPE OF USERS? *LARRY WELKE, INTERNATIONAL COMPUTER PROGRAMS*
MARKETING COMMUNICATIONS		PUSHING THE LIMITS OF CREATIVITY IN MARKETING *CAMILLE SCHUSTER, VIRGINIA POLYTECHNIC INSTITUTE AND STATE UNIVERSITY*	EVALUATING AND SELECTING AGENCY COMPUTER SYSTEMS	VIDEOTEX *RONALD SOLBERG, CONTINENTAL BANK*	DIRECT MARKETING: TARGETING CUSTOMERS THROUGH THE USE OF SPECIALIZED DATABASES *PAUL WARREN, MAGNA TEX INTERNATIONAL LTD*
ENGINEERING (CAD/CAM/CAE)					
COST ANALYSTS					

JUNE 17		WEDNESDAY JUNE 18			
1:30-3:00 PM	3:30-5:00 PM	8:30-10:00 AM	10:30 AM-12:00 PM	1:30-3:00 PM	3:30-5:00 PM
	DEREGULATION AND AUTOMATION—THE FINANCIAL INDUSTRY *JOHN PARADY, BANK OF AMERICA*	TRENDS IN CONTRACT SERVICES *PHILIPPE DREYFUS, CAP GEMINI SOCIETY, PARIS*	COMPUTER POLITICS AND POLICIES *JOHN GOSDEN, THE EQUITABLE*	AN EXPERT PREDICTS THE FUTURE *ALAN PALLER, AUI DATA GRAPHICS/ISSCO*	
CHIEF INFORMATION OFFICER—SUCCESS OR FAILURE *NANCY MARKLE, ARTHUR YOUNG*			INFORMATION-CENTER CASE STUDY—MEASURING SUCCESS *JEROME THODE, DELOITIE, HASKINS & SELLS*		
	ARE VDTs INJURIOUS TO YOUR HEALTH? *BONNIE JOHNSON, AETNA LIFE AND CASUALTY*	CAN/SHOULD DATA PROCESSING CONTROL PC AND INFORMATION-CENTER ARCHITECTURE AND USAGE? *PAUL ROSENTHAL, COOPERS & LYBRAND*		DOES OUR FORMAL EDUCATION SYSTEM MEET THE NEEDS OF COMPUTER PROFESSIONALS AND THEIR EMPLOYERS? *JOHN SCHLEICH, UNIVERSITY OF NEVADA*	IS TRANSBORDER DATA CONTROL A PRIVACY OR A POLITICAL-ISOLATIONISM ISSUE? *TERRY CURTIS, CALIFORNIA STATE UNIVERSITY AT CHICO*
THE FUTURE OF CAD/CAM PRODUCTIVITY *JOSEPH HARRINGTON, ARTHUR D LITTLE*	LIFECYCLE DATABASES FOR BUILDINGS *CURTIS POUNDS, McDONNELL-DOUGLAS ARCHITECTURAL, ENGINEERING & CONSTRUCTION SYSTEMS CO*	GRAPHICS WORKSTATION TECHNOLOGY TRENDS *CARL MACHOVER, MACHOVER ASSOCIATES*	HOW MUCH COMPUTER FOR THE ANALYTICAL JOB? *J E BLOUIN, McDONNELL-DOUGLAS ISG*		
		DECISION-SUPPORT SYSTEMS—MYTH OR REALITY? *OSCAR BILODEAU, HUMPHREYS AND ASSOCIATES*	ARE VPs AND PCs COMPATIBLE? *GEORGE ROCK, TELEDYNE SYSTEMS*	ARE GOVERNMENT FINANCIAL REPORTS REALLY NECESSARY?	BEAN COUNTER OR FINANCIAL DATA COMPILER AND INTERPRETER? *DICK GOVEN, ROCKWELL INTERNATIONAL*

Continued on pg 154

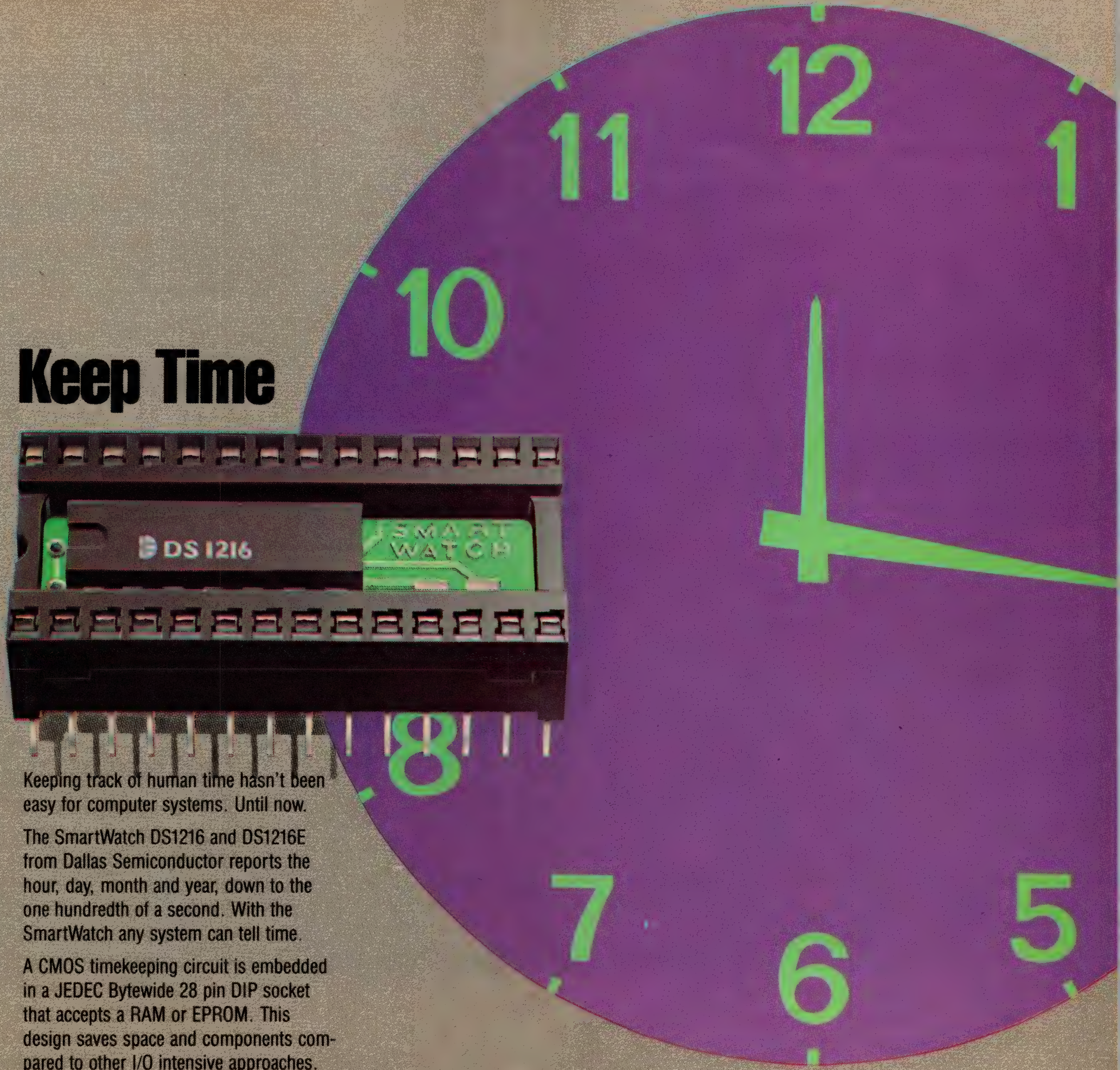
NCC '86 COMPLIMENTARY SESSIONS (THURSDAY JUNE 19)

	8:30 - 9:15 AM	9:15 - 10:00 AM	10:00 - 10:45 AM	10:45 - 11:30 AM	11:30 AM - 12:15 PM	1:00 - 1:45 PM	1:45 - 2:30 PM
RESEARCH AND DEVELOPMENT IN THE COMPUTER INDUSTRY	SOME PROBLEMS NEITHER MY COMPUTER NOR I CAN SOLVE . . . YET	APPLYING SOFTWARE RELIABILITY MODELS TO DECISION SUPPORT	NONCHRONOLOGICAL SEQUENTIAL SIMULATION	DETECTING LOOP STRUCTURE IN ASSEMBLY CODE	PROJECT SOURCE-FILE MANAGEMENT UNDER THE UNIX OPERATING SYSTEM	FAULT TOLERANCE AND DIAGNOSABILITY OF A CLASS OF BINOMIAL INTERCONNECTION NETWORKS	PARALLEL PROBABILISTIC COMPUTING
	IDENTIFICATION, AUTHENTICATION, AND PRIVACY IN DIGITAL COMMUNICATIONS	UPDATES IN RELATIONAL DATABASES	SPQL: SOFTWARE PRODUCT QUALITY LEVEL	EXTENDING THE CAPABILITIES OF WORD-PROCESSING SOFTWARE	GENERATION OF MINIMUM TEST SETS FOR DETECTION AND LOCATION OF MULTIPLE FAULTS IN FANOUT-FREE COMBINATION CIRCUITS	GRAPH-THEORETIC BOUNDS FOR ON-LINE CHECKS IN MULTIPLE-PROCESSOR SYSTEMS	HOW TO CONVERT INFORMAL IDEAS TO FORMAL IDEAS IN SOFTWARE ENGINEERING
SMALL-BUSINESS COMPUTING	8:30 - 10:00 AM	10:30 AM - 12:00 PM	1:30 - 3:00 PM	3:30 - 5:00 PM			
	HOW TO KNOW YOU'RE READY FOR AUTOMATION	HOW TO STREAMLINE YOUR COMPUTER PURCHASE	HOW TO MAKE YOUR COMPUTER WORK FOR YOUR BUSINESS	INSIDE INFORMATION FROM FIRST-TIME USERS			

NCC '86 PROFESSIONAL-DEVELOPMENT SEMINARS

SUNDAY JUNE 15	MONDAY JUNE 16	TUESDAY JUNE 17	WEDNESDAY JUNE 18			THURSDAY JUNE 19
1:00-4:30 PM	1:00-4:30 PM	8:30 AM-4:30 PM	8:30 AM-12:00 PM	8:30 AM-4:30 PM	1:00-4:30 PM	8:30 AM-4:30 PM
THE ONE-MINUTE MANAGER: PUTTING IT TO WORK FOR YOU	AN EXECUTIVE BRIEFING BY TOP WOMEN	SUCCESSFUL PROJECT PLANNING AND MANAGEMENT: STATE-OF-THE-ART STRATEGIES	BUILDING EXPERT SYSTEMS	DEALING WITH DIFFICULT EMPLOYEES	ENTRE AND INTRA PRENEURING IN THE USA TODAY: METHODS, TACTICS, AND FRIENDS	HOW TO COMMUNICATE MORE EFFECTIVELY
SUPERCOMPUTERS: A ROUND TABLE DISCUSSION	TYPES OF DISASTERS THAT COULD OCCUR AND THE IMPACT THEY COULD HAVE ON YOUR BUSINESS	AN ARTIFICIAL-INTELLIGENCE WORKSHOP	USING MICROGRAPHICS FOR EFFECTIVE BUSINESS PRESENTATIONS (HANDS-ON)	LOCAL-AREA-NETWORK REQUIREMENTS AND SOLUTIONS	EXPERT SYSTEMS (HANDS ON)	COMPUTER-INTEGRATED MANUFACTURING AND ROBOTICS
THE TEAM APPROACH TO DISASTER-RECOVERY PLANNING	LINKING PEOPLE AND TECHNOLOGY	LOGICAL DATA MODELING/DATA ANALYSIS		PROACTIVE MANAGEMENT OF TECHNOLOGICAL CHANGE AND CONFLICT		IMPLEMENTING A DATA CENTER IN AN ON-LINE ENVIRONMENT
THE TEN MOST ENDURING MANAGEMENT PRINCIPLES	BUSINESS AND PROFESSIONAL WRITING	SELLING TO TOP MANAGEMENT THE NEED FOR A CORPORATE CONTINGENCY PLAN		HIGH-TECH BUSINESS PLANNING AND MONEY		PROJECT-MANAGEMENT SURVIVAL COURSE
THE CHANGING ROLE OF THE DATA-PROCESSING PROFESSIONAL	TECHNOLOGY'S IMPACT ON CORPORATE CULTURE	ASSERTIVE MANAGEMENT AND EFFECTIVE LEADERSHIP		THE ART OF NEGOTIATING FOR THE DATA-PROCESSING PROFESSIONAL		MANAGING MULTICULTURAL ENVIRONMENT
	ENHANCED USES OF DBASE III (HANDS ON)	COMPUTER LAW FOR THE DATA-PROCESSING PROFESSIONAL				IMPLEMENTING NEGOTIATION PRINCIPLES FOR THE DP PROFESSIONAL
	COMPUTER CRIME	LOTUS 1-2-3 ADVANCED TECHNIQUES WORKSHOP (HANDS ON)				SOFTWARE DEVELOPMENT UNDER UNIX (HANDS ON)

Keep Time



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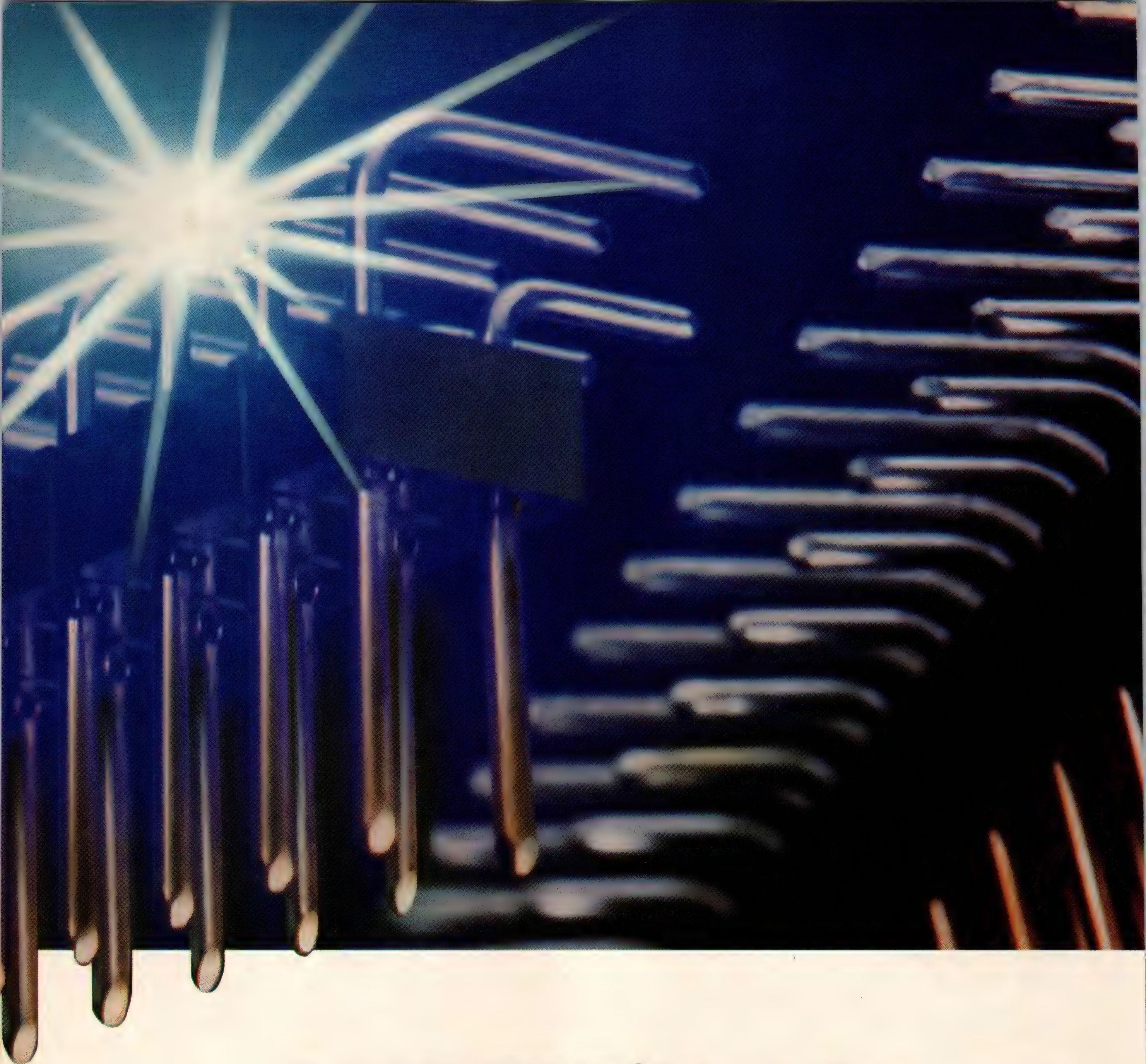

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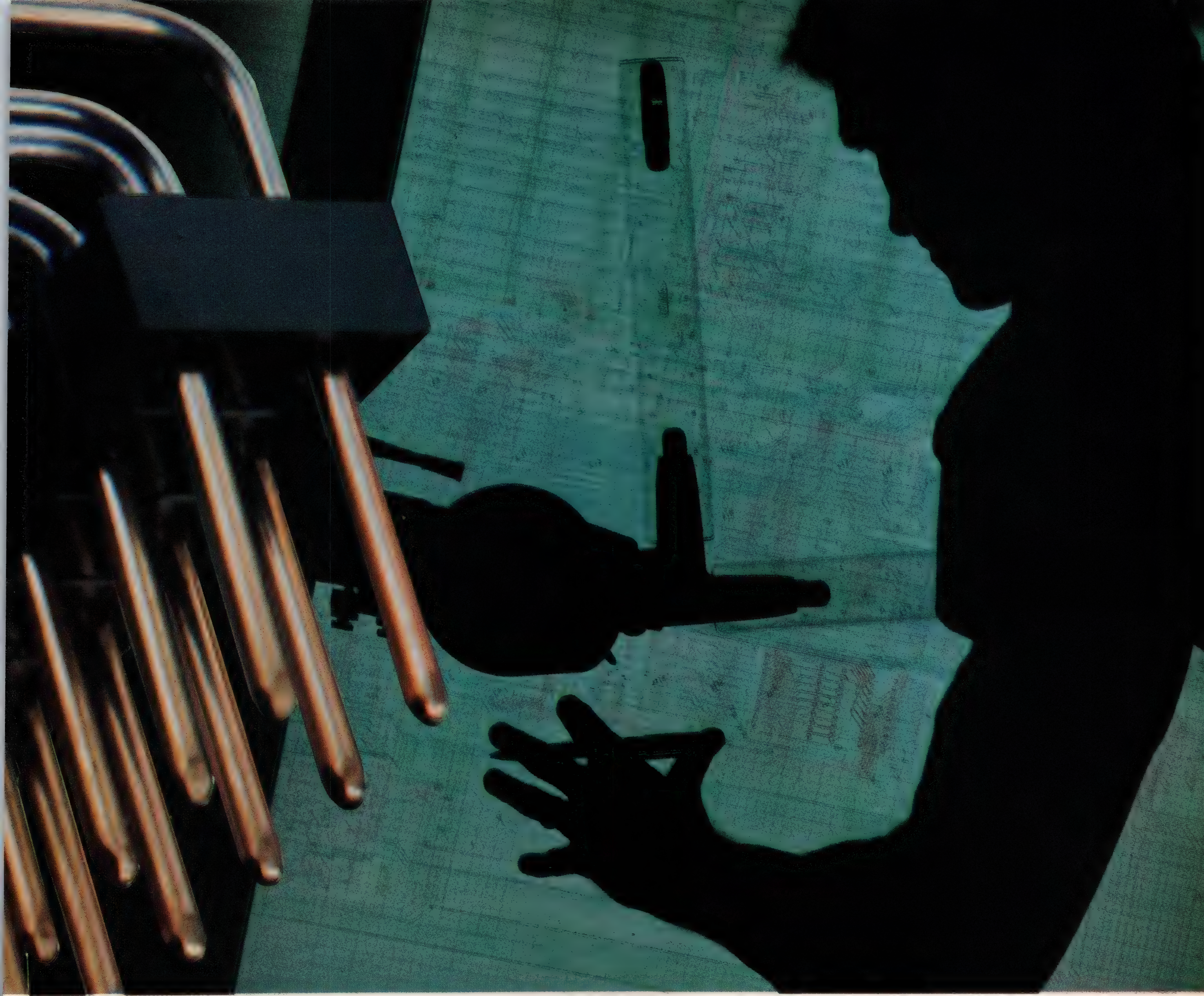

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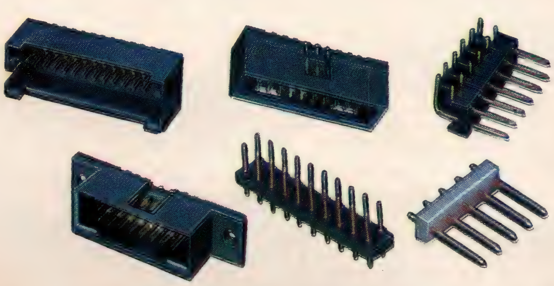

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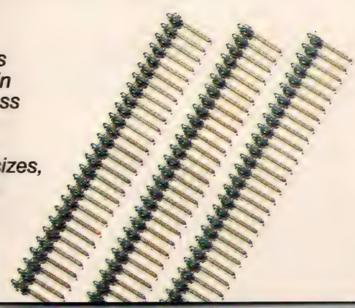

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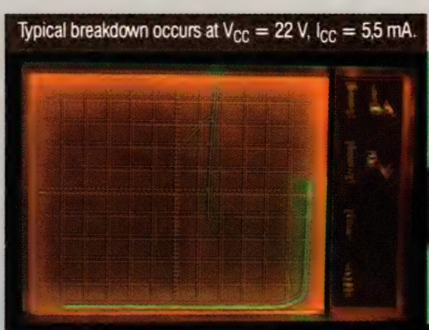
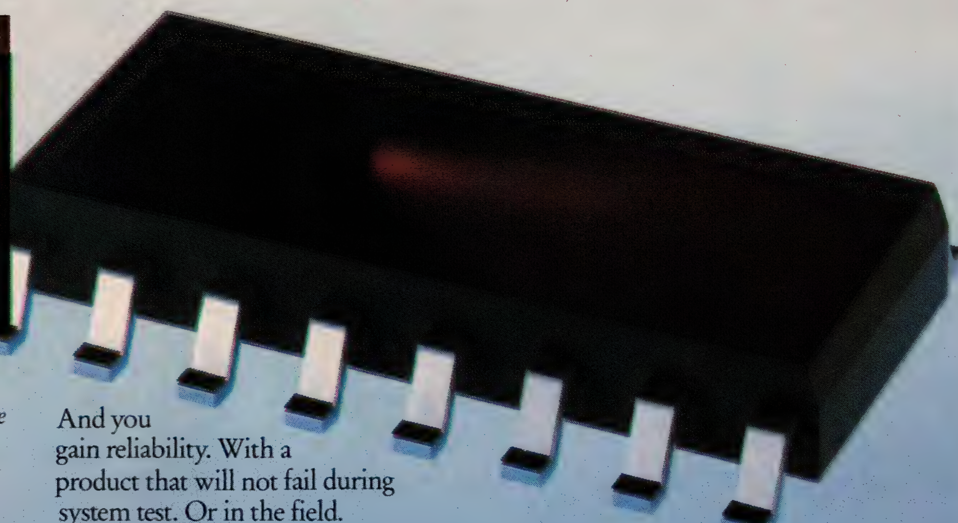


Curve tracer display from latch-up test with excess supply voltage. At no time did latch-up occur in the Philips HCMOS IC, since the supply voltage snaps back to 13 V.



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CIRCLE NO 107

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Timing verification predicts performance of logic arrays

You can determine the dynamic performance of your logic-array design using timing-verification techniques. Once you have models of the signal propagation delays characteristic of logic arrays, you can investigate the ac parameters of your design by using a logic simulator and several types of analyses.

Michael Franz, *Applied Micro Circuits Corp*

Before committing your logic-array design to fabrication, it's possible to ascertain its dynamic performance. Using a logic simulator with timing analysis, you can measure ac performance parameters such as propagation delay, setup-and-hold (SUH) times, and worst-case maximum system frequency. You can monitor these parameters as a function of variances in operating temperature, supply voltage, and process variations, factors you encounter with the physical implementation of your design.

When you tackle the timing analysis of a circuit you are dealing with physical phenomena such as rise time, fall time, and trigger points—albeit at some level of abstraction. A circuit model of these phenomena would constitute a complex set of nonlinear differential equations. Timing analysis at the circuit level would be cumbersome, but ignoring any analysis can be lethal to your design.

Hence, you need a simple model, one that makes computations of logic timing easy, understandable, and expedient. At the same time, the model must predict the dynamic behavior of your circuit accurately. The following examples illustrate the development of one such model commonly used in timing analysis.

All timing simulations investigate the effect of internal signal delays on the overall performance of a logic array. Delays are categorized as macro-internal (intrinsic) or loading (extrinsic) delays. Furthermore, extrinsic delays depend on the load-driving capability of the circuitry (drive factor) and the amount of load on the circuit macro (load factor).

In any logic array, signals enter at input pins where buffers translate the external signal levels (eg, TTL, ECL, CMOS) to internal signal levels. Logical operations occur in a series of macros, which modify the primary input signal through logic combinations (such as AND operations, OR operations, and inverting operations) with other signals. Each macro delays the propagation of the input signal to the output pin.

Illustrating the delay accumulation, a logic-array signal path appears in **Fig 1.** The delay from the input of the driver to the input of the receiver constitutes an intrinsic delay t_{IN} and an extrinsic delay t_{EX} (also known as loading delay).

There is a qualitative difference between these two delays. Although the internal delay is a fixed delay

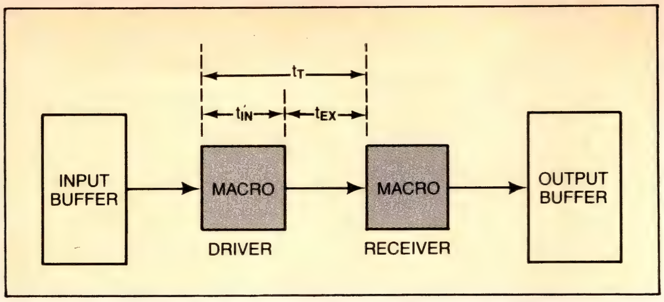

***Fig 1—Propagation delay through a logic array** depends on the internal (intrinsic) delay of the macros in the design and on the load (extrinsic) delay between the macros.*

caused by circuitry that postpones the occurrence of a signal transition, the external delay is a construct. It's proportional to the load capacitance seen by the output of the driver. As capacitance increases, the magnitude of the slope of the curve representing driver output vs time decreases **(Fig 2)**, which increases the elapsed signal delay before the signal voltage crosses the trigger voltage of the receiver.

The total signal delay t_T, therefore, is the sum of the intrinsic (t_{IN}) and extrinsic (t_{EX}) delays:

$$t_T = t_{IN} + t_{EX}.$$

Logic-array vendors characterize intrinsic delays and publish them in macro specification sheets. These delays are not dependent on the logic or layout context in which you use the macro.

Extrinsic delays, in contrast, are dependent on the logic and layout environment of the particular macro. Fortunately, chip dimensions are still small enough (compared to the wavelengths of the highest frequencies of most chip designs) that you can lump all loading on a particular macro into one capacitance. Consequently, you don't have to consider transmission-line effects; instead, you add all load capacitance, together with the associated load delays, regardless of their location relative to the driving macro:

$$t_{EX} = \Sigma t_{EX,N},$$

where $t_{EX,N}$ represents the individual load-delay contributions.

The two main causes of loading delays are fan-out and interconnect wiring. In fan-out loading, all driven inputs constitute a loading capacitance (in addition to a resistive load in bipolar circuits). Interconnect loading results from the one or two layers of metal used to interconnect circuits on the chip. All wiring in metal layers contributes to the load capacitance.

An additional contribution to extrinsic delays comes from circuit structures particular to certain technologies: wired-AND, wired-OR, and bus logic add to the loading delay because the outputs of the connected drivers contribute capacitance. When you consider this third contribution,

$$t_{EX} = t_{FO} + t_{WIRE} + t_W,$$

where t_{FO} is the fan-out load contribution, t_{WIRE} is the interconnect-wiring load contribution, and t_W is the load contribution from other technology-dependent loads. ECL circuitry, for example, can implement wired-OR macro outputs. Each additional output driving the wired-OR circuit introduces additional load capacitance.

As you design a logic array, you define with increasing accuracy loading contributions at different points in the design process. You define the fan-out and wired logic delays when you finish your net list, and you can incorporate these delays in your logic simulations. The simulations can establish the functionality and (not counting wiring delays) the timing of your circuit. The interconnect wiring, which can introduce a substantial delay, is at this point undetermined, so your timing simulations do not accurately reflect the signal timing of your finished chip.

To model extrinsic delays, you lump the logic- and layout-dependent load capacitance in one load, L, expressed in terms of load units, LU. You use this representation (instead of using capacitance expressed in pF) because it simplifies your delay calculations. All loading delays are therefore the product of a drive factor k (the driving capability of the driving macro) and the sum of all loads (L_i) in the driven net. For instance, consider the following equation:

$$t_{EX} = k(L_{FO} + L_{WIRE} + L_W),$$

where L_{FO} is the fan-out load, L_{WIRE} is the interconnect-wire load, and L_W represents technology-dependent loads, such as wired-OR logic. The drive factor, k, is a property of the individual output of a macro; you find it in the logic-array vendor's data sheets. The units for k are nsec/LU.

Typically, the value of k for a low-high transition differs from that for a high-low transition because current-sinking and current-sourcing capabilities of outputs are usually asymmetric. Thus, the extrinsic delay, t_{EX}, typically differs for the two transitions:

$$t_{EX,UP} = k_{UP} \cdot \Sigma L_I, \text{ and}$$
$$t_{EX,DOWN} = k_{DOWN} \cdot \Sigma L_I,$$

where L_I represents the individual load contributions.

Timing analysis of the circuit in **Fig 3** includes a wired-OR-load and an asymmetric-drive factor. L_{FO} is the sum of all input loads connected to the driven net. The first receiver input has a load of 2 LUs and the

The extrinsic delay is a construct; it's proportional to the load capacitance seen by the output of the driving macro.

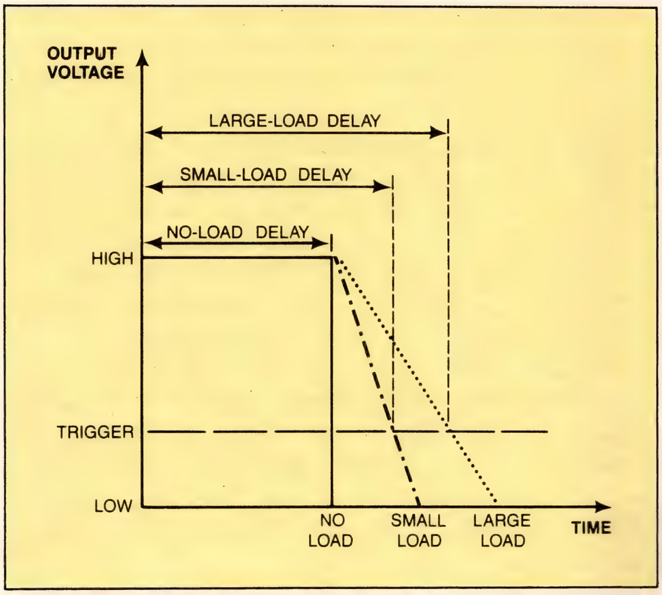

Fig 2—Extrinsic delay increases with macro loading. *An unloaded macro exhibits little or no extrinsic delay. Adding load increases the slope of the macro's output waveform, thereby increasing the extrinsic delay.*

second has a load of 1 LU, so L_{FO}=3 LUs. The wire load due to the net is directly proportional to the length of the wire segments l_{WIRE} in first- and second-layer metal:

$$L_{WIRE}=L_{WIRE1}+L_{WIRE2}$$
$$=Q_{WIRE1}l_{WIRE1}+Q_{WIRE2}l_{WIRE2},$$

where Q_{WIRE} represents the wire load of interconnecting metal in LU/mm.

For 0.5 mm of first-layer metal and 0.8 mm of second-layer metal in **Fig 3,** and for wire loads of Q_{WIRE1}=3.2 LU/mm and Q_{WIRE2}=1.5 LU/mm, the total wire load is

$$L_{WIRE}=3.2\cdot0.5+1.5\cdot0.8=2.8\ \text{LU}.$$

Two circuit macros drive the driven net, creating a wired-OR circuit. The load on wired-OR circuits is the sum of the possible driving macros (n) minus the one actually driving the net, multiplied by a wired-OR driving factor, W.

$$L_W=W\cdot(n-1).$$

Using k_{UP}=0.04 nsec/LU (low-to-high driving factor), k_{DOWN}=0.11 nsec/LU (high-to-low), and W=1 LU, the total typical delay for the example in **Fig 3** becomes

$$t_{EX,UP}=0.04\cdot(3+2.8+1)=0.27\ \text{nsec},$$
$$t_{EX,DOWN}=0.11\cdot(3+2.8+1)=0.75\ \text{nsec}.$$

Operational, process factors have effect

Delays on a logic array depend on a variety of operational and manufacturing parameters. Specifically, temperature and supply voltage directly affect the magnitude of delays. Furthermore, processing parameters introduce uncertainty factors into calculations. Luckily, chip dimensions are small enough that you can consider these influences as uniform across all circuitry on the chip.

The most pronounced deviation of propagation delays results from variations in operating conditions. Chip temperature and supply voltage can vary within specified ranges for commercial- or military-grade applications. These ranges form a window of operation; as long as your chip operates within this window, the logic-array vendor guarantees that it will meet its performance requirements.

Within the window, however, performance does vary with temperature and voltage supply. In most cases, performance improves as the supply voltage increases and the ambient temperature drops. However, exceptions that depend on the circuit and process technology do exist. At any point in the operating window, you can use a performance modifier to increase or decrease all delays subject to the particular operating condition. The performance modifier under typical operating conditions, M_{TYP}, equals 1.

The performance modifier multiplies the total delay

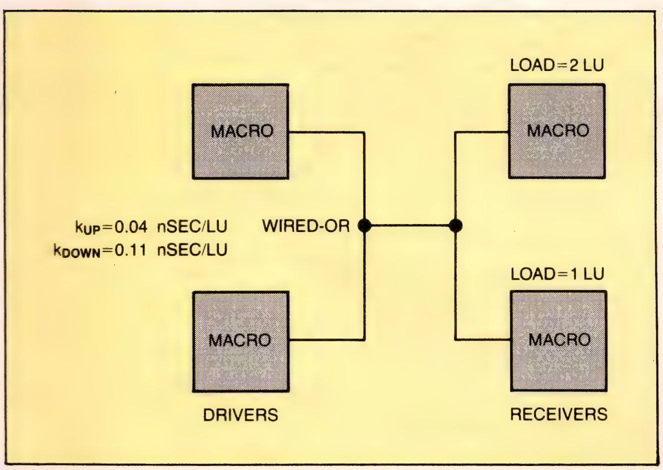

Fig 3—Wired-OR circuitry adds signal delay *to the total propagation delay. In this example, as in many circuits, the drive factor for upward transitions is different from the drive factor for downward transitions.*

Temperature and supply voltage directly affect the magnitude of delays; processing parameters introduce uncertainty factors into calculations.

of a macro to produce the modified delay $t_{T,M}$:

$$t_{T,M}=M \cdot t_T=M \cdot t_{IN}+M \cdot t_{EX}.$$

The equation for $t_{T,M}$ reveals three characteristics of the performance modifier: First, it modifies the intrinsic and the extrinsic delay of a macro equally. Second, it affects the low-high and the high-low transitions equally. Third, it has the same effect on all macros on a chip. Although these characteristics simplify the physical response of the chip to operational variations, they're justified by the resulting simplification of the calculations.

The performance modifier's third characteristic, in addition, is based on intuition. Temperature and voltage differences among all points on a chip are small, and the chip and its package are good heat conductors that tend to equalize temperature across the chip. Moreover, all on-chip devices connect to the same power bus. Consequently, all macros respond similarly to temperature and voltage fluctuations (called on-chip tracking).

Another parameter affecting delay on all devices on a chip uniformly is fluctuation of the manufacturing process. The logic-array vendor controls this fluctuation with narrow limits and sets a guardband around the value of the performance modifier to compensate for process variations.

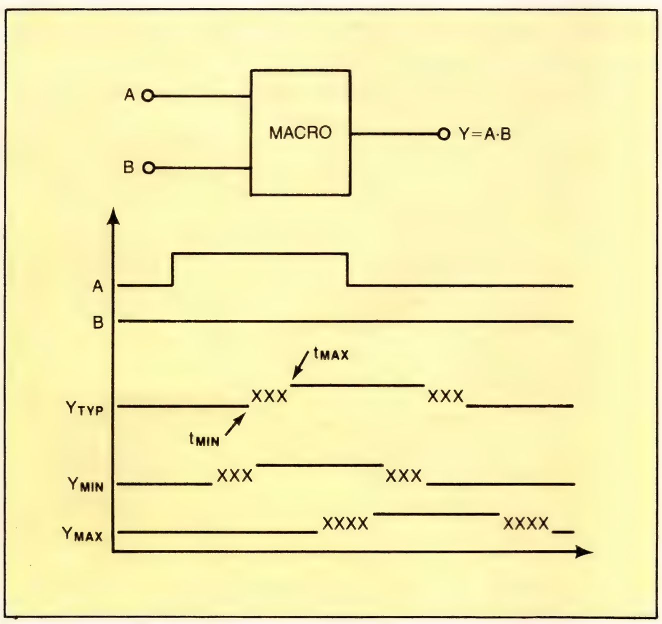

Fig 4—Ambiguity in signal propagation delay *results from random and uncontrollable factors such as process variations and crystal defects. The state X represents propagation ambiguity.*

In most cases, logic-array vendors don't publish modifiers for every combination of voltage and temperature at which they specify chip performance. Instead, they supply values of M that represent the most extreme operating conditions. Then, if a logic design proves viable under typical operating conditions ($M_{TYP}=1$) as well as at extreme conditions (eg, $M_{MIN}=0.7$ and $M_{MAX}=1.45$), you can assume that the design functions within the entire operating range.

On-chip tracking allows more aggressive dynamic design (particularly valuable in a high-speed operating environment) than is possible on a pc board where temperature and supply-voltage variations are more pronounced. Also, ICs on any one pc board rarely all come from the same manufacturer and, even less likely, from the same manufacturing lot. The chips' dynamic performance doesn't track as closely as devices on a logic array.

Unfortunately, other physical phenomena cause random or uncontrollable performance fluctuations across the chip. First, chip anomalies such as crystal defects, local mask defects, and local contamination cause random variations. A second category is uncontrollable by the logic designer: Variations in power-bus voltage, temperature hot spots, and characterization inaccuracies, for example, cause performance to deviate from the typical performance for a given operating condition. For a well-characterized array-design system, these random and uncontrolled performance deviations shouldn't exceed 10%.

The resulting timing model separates the on-chip tracking from the random and uncontrollable performance variation. To illustrate, **Fig 4** shows the timing model for a 2-input AND gate. The output, Y, follows the input, A, after a certain delay. Random and uncontrollable variations cause the actual transition time to be uncertain; the state X reflects the period of uncertainty. You can be positive that the transition will occur no earlier than t_{MIN} and no later than t_{MAX}. The Y_{TYP} waveform models this phenomenon under typical operating conditions, eg, T=25°C and V_{CC}=5V.

In contrast, Y_{MIN} and Y_{MAX} represent the same output under the predictable minimum- and maximum-delay operating conditions. When you include all performance modifiers, you encounter many timing-model equations:

$$t_{T,MIN,MIN}=t_T M_{MIN}(1-A)$$
$$t_{T,MIN,TYP}=t_T M_{MIN} \cdot 1$$
$$t_{T,MIN,MAX}=t_T M_{MIN}(1+A)$$

$$t_{T,TYP,MIN}=t_T \cdot 1 \cdot (1-A)$$
$$t_{T,TYP,TYP}=t_T \cdot 1 \cdot 1$$
$$t_{T,TYP,MAX}=t_T \cdot 1 \cdot (1+A)$$
$$t_{T,MAX,MIN}=t_T M_{MAX}(1-A)$$
$$t_{T,MAX,TYP}=t_T M_{MAX} \cdot 1$$
$$t_{T,MAX,MAX}=t_T M_{MAX}(1+A).$$

Don't be confused by the profusion of delay equations. They indicate that, for each of the three operating conditions, MIN, TYP, and MAX, you can assume that the propagation delay will have an accuracy of $\pm A \cdot 100\%$, where A is the transition ambiguity caused by random and uncontrollable variations.

Once you've developed a timing-analysis model, you can move on to a logic simulator. A logic simulator performs actual timing verification. You enter a description of your circuit, models for circuit delay, and input waveforms to the simulator. The simulator can then examine system delays, interval checks, SUH times, and minimum and maximum performance, as well as external SUH times. (For an introduction to logic simulation and simulation vectors, see "Designers Guide to: Simulation and test vectors," EDN, June 13, 1985, pg 153, and June 27, 1985, pg 233.)

A logic simulator applies the desired input waveforms to the inputs of your circuit. It then determines the response of input macros to the waveforms and applies that response to logic macros that are connected to the input macros. In this way, the effect of the input waveforms propagates through your logic design to the outputs of the net list. As the simulator calculates the response of macros to propagating waveforms, it can incorporate timing information into the response.

In its simplest form, a logic simulator simply adds each propagation delay to a signal's total delay as it propagates through a net list. For example, the two positive-edge-triggered flip-flops in **Fig 5** form a shift register. The input stimuli at internal node Q_1 and the signal at output node Q_2 appear in the accompanying wave diagram.

The flip-flops have a clock-to-output delay of 2 nsec typ for both transitions of Q (low-to-high and high-to-low). The total loading delay on FF_1 amounts to 0.2 nsec for both transitions, and FF_2 has no load. On the rising edge of the clock at t=10 nsec, FF_1 initializes at time 10+2+0.2=12.2 nsec. FF_2 initializes one clock period later at 32.0 nsec. The Xs on the Q_1 and Q_2 waveforms indicate that the states of the flip-flop outputs are initially unknown. This timing simulation predicts the typical delay through the circuit.

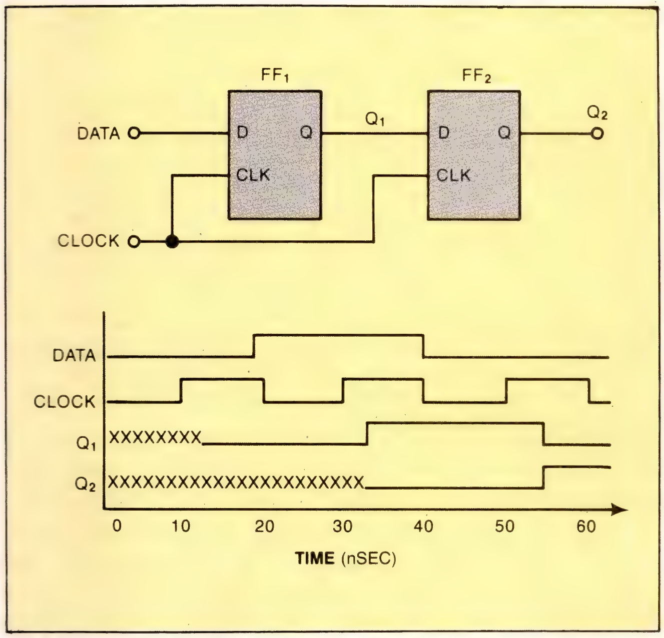

*Fig 5—**Determine the worst-case propagation delay** by using a simulator to perform basic path-delay calculations. The simple shift register shown initializes the first flip-flop at t=12.2 nsec and the second flip-flop at t=32 nsec.*

To check for worst-case performance, you apply the same input stimuli with the delay parameters adjusted to maximum or minimum delay. Some simulators allow the global multiplication of all typical delay values by a worst-case-performance factor. Then you can use the multipliers M_{MAX} and M_{MIN} to simulate your circuit's operation under extreme operating conditions.

Most logic simulators can detect and report the existence of unwanted pulses in propagating signals (pulse shaping). Such pulses (also called spikes or glitches) occur when a signal's state is shorter than the propagation delay of a macro. A race condition exists when a gate's inputs switch simultaneously or almost simultaneously, causing the gate output to change state in rapid succession before it reaches its final state. The simulator typically produces an undefined state X at the macro output for the duration of the pulse; you should eliminate the cause of spikes when you see that output, particularly on clock, set, or reset signals.

Many logic simulators have provisions that let you check for proper timing of signals relative to other signals. For instance, you may want to verify SUH times and pulse-width requirements for the macros in your circuit. If signals in your simulation violate the SUH or pulse-width specifications set by the logic-array vendor, the simulator issues a warning to that

For each of the three operating conditions, MIN, TYP, and MAX, you can assume that the propagation delay has an accuracy of ±A·100%.

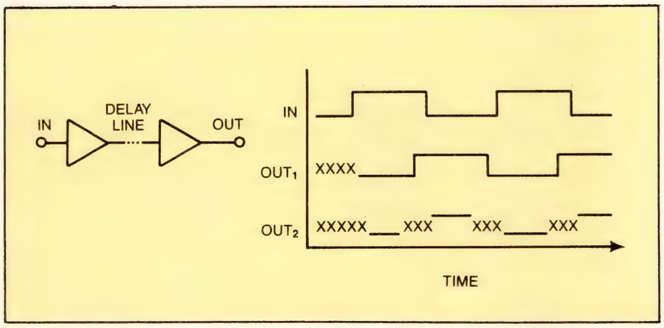

Fig 6—Simulators should propagate transitional ambiguity *to reveal possible signal degradation resulting from random and uncontrollable variations in performance. Such ambiguity is represented here in OUT_2, but not in OUT_1.*

effect. Simulating with these checks allows you to get accurate estimates of chip-performance parameters.

To illustrate one such estimate, the circuit in **Fig 5** exhibits a maximum operating frequency inversely proportional to the sum of the set up time of FF2 and the maximum delay from the clock input to the output of FF_1. Given the stated delays and $M_{MAX}=1.4$, the maximum delay is 1.4·(2+0.2 nsec)=3.08 nsec, and the maximum operating frequency becomes 1÷3.08 nsec=325 MHz. However, if you include a set up time of 1 nsec for FF_2, the maximum operating frequency drops to 1÷(3.08+1)=245 MHz. If you simulate your circuit on a simulator that checks SUH times, increasing the operating frequency above 245 MHz results either in erroneous results or a warning statement from the simulator.

Simulators that model only signal-delay and timing checks may not be able to simulate transitional ambiguity. For example, the output OUT_1 of the delay line in **Fig 6** shows the waveform from a timing analysis without transitional ambiguity. Clearly, OUT_1 doesn't include the uncertainty associated with the transitions of the output of the delay line. A simulator that can simulate minimum and maximum transition delays (a minimum/maximum simulator) models the transitional ambiguity that appears in OUT_2.

OUT_2 exhibits the expected delayed input signal A and the transition areas displayed as the state X. During the transition, the value of signal OUT_2 is unknown, but the signal transition occurs somewhere during the X window. Consequently, the pulse may grow as large as from the first X of an upward transition to the last X of a downward transition. Conversely, the pulse may shrink to the period between the last X of the upward to the first X of the downward transition. The minimum/maximum simulation reveals the possible signal degradation (pulse shaping) resulting from random and uncontrollable variance in logic-array performance.

Unfortunately, this type of minimum/maximum simulation is accurate only as long as interacting signals are independently generated. Most logic-array circuits, however, contain dependent, interacting signals whose interaction is called reconvergent fan-out. In the circuit of **Fig 5**, two sets of interacting signals—Clock and Q_1 (which is the data input of FF_2) and clock and data inputs of FF_2—have a common origin or cause (Clock). Therefore, any ambiguity existing in the Clock signal doesn't have an effect on the timing of the two interacting (reconverging) signals, because it's common to both.

Fig 7 depicts a situation in which a minimum/maxi-

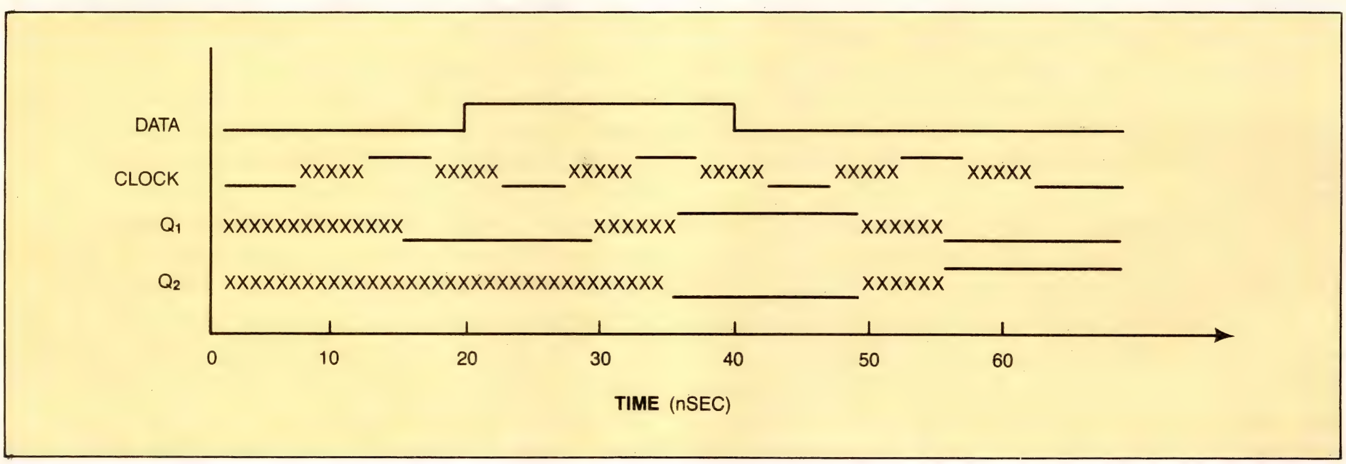

Fig 7—These waveforms, *similar to those in* ***Fig 5,*** *depict a situation in which a minimum/maximum simulator might generate incorrect output resulting from reconvergent fan-out.*

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Most logic simulators can detect and report the existence of unwanted pulses in propagating signals (pulse shaping).

mum simulator might generate incorrect output resulting from reconvergent fan-out. The waveforms are the same as those in **Fig 5** except that the transitional ambiguity in the Clock signal appears when the Clock signal changes. The incorrect output arises at t=30 nsec when the clock input stores the value of Q_1 into FF_2. Most minimum/maximum simulators will flag a set-up violation because the Clock signal can change during the ambiguity period of the data input, Q_1. If Clock goes high at the leading edge of the period, the value at Q_1 latches properly, but if Clock goes high at the trailing edge of the period, the value at Q_1 doesn't latch. If Clock and Q_1 are independent signals, (eg, primary input signals) this SUH violation would be accurate because Clock may or may not occur soon enough to store Q_1.

In this example, however, the occurrence of the data transition results from an occurrence of a Clock transition. An interaction of the front clock edge with the tail data edge isn't possible (not considering a possible ambiguity in Q_1 from the macro delay). The waveforms in **Fig 7** are possible only via a minimum/maximum simulation capable of resolving reconvergent fan-out. In effect, this simulation removes the common ambiguity of two interacting signals and reinserts it at the resulting output. Good simulators can trace signals back to primary inputs to detect common signal origins and to remove common ambiguity at a point of reconvergence.

Verify setup-and-hold times

Once you know the SUH times of circuits in your design, it's desirable to be able to verify them when you receive your prototypes. Because you only have access to your I/O signals (at the pins of your IC), you must determine SUH times in reference to those signals. For example, the flip-flop in **Fig 8** is stimulated by the Data and Clock input signals (referred to as primary inputs). The circuitry between the primary inputs and the flip-flop introduces delays t_D and t_C that you must compensate for in your SUH calculations for the flip-flop.

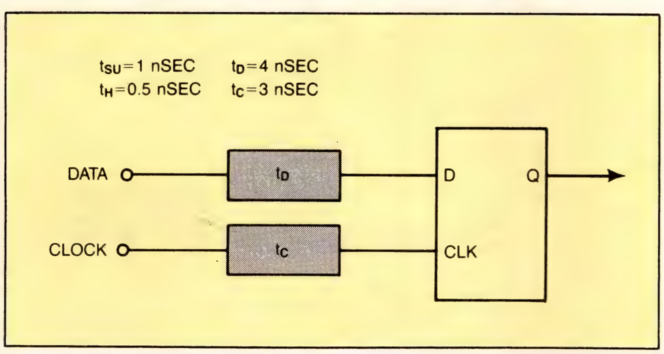

Fig 8—Intervening circuitry changes SUH times *for this flip-flop. You must include the propagation-delay effects of the Clock and Data signal paths to determine the external SUH times at the primary input signals.*

Given the worst-case SUH times (t_{SU} and t_H) of the internal flip-flop, external setup time $t_{SU,EX}$ is

$$t_{SU,EX}=t_{SU}+t_D-t_C,$$

and the external hold time $t_{H,EX}$ is

$$t_{H,EX}=t_H+t_C-t_D.$$

The situation becomes more complicated when you include the effect of operating conditions. Considering the performance modifiers, the SUH times (under worst-case conditions) become

$$t_{SU,EX}=t_{SU}+M_{MAX}(t_D-t_C),\ t_D>t_C$$
$$t_{SU,EX}=t_{SU}+M_{MIN}(t_D-t_C),\ t_D<t_C$$
$$t_{H,EX}=t_H+M_{MAX}(t_C-t_D),\ t_C>t_D$$
$$t_{H,EX}=t_H+M_{MIN}(t_C-t_D),\ t_C<t_D.$$

Finally, if you consider the transition ambiguity, the external SUH equations are

$$t_{SU,EX} = t_{SU} + M_{MAX}\,[t_D(1 + A) - t_C(1 - A)],$$
$$t_D(1 + A) > t_C(1 - A)$$
$$t_{SU,EX} = t_{SU} + M_{MIN}\,[t_D(1 + A) - t_C(1 - A)],$$
$$t_D(1 + A) < t_C(1 - A)$$
$$t_{H,EX} = t_H + M_{MAX}\,[t_C(1 + A) - t_D(1 - A)],$$
$$t_C(1 + A) > t_D(1 - A)$$
$$t_{H,EX} = t_H + M_{MIN}\,[t_C(1 + A) - t_D(1 - A)],$$
$$t_C(1 + A) < t_D(1 - A).$$

In **Fig 8**, the worst-case external SUH times are, assuming M_{MAX}=1.4, M_{MIN}=0.7, and A=10%,

$$t_{SU,EX}=1.0+1.4(4\cdot1.1-3.0\cdot0.9)=3.38\text{ nsec}$$
$$t_{H,EX}=0.5+0.7(3.0\cdot1.1-4.0\cdot0.9)=0.29\text{ nsec.}$$

In this example, clock- and data-path delays lengthen the minimum required data pulse considerably, from 1.5+0.5=2 nsec to 3.38+0.29=3.67 nsec.

The most accurate timing simulation is possible after you determine the layout of your logic array. At this point, all macros have been placed on the chip and all

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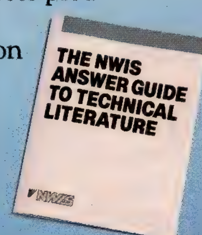

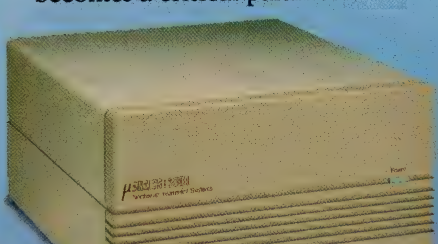

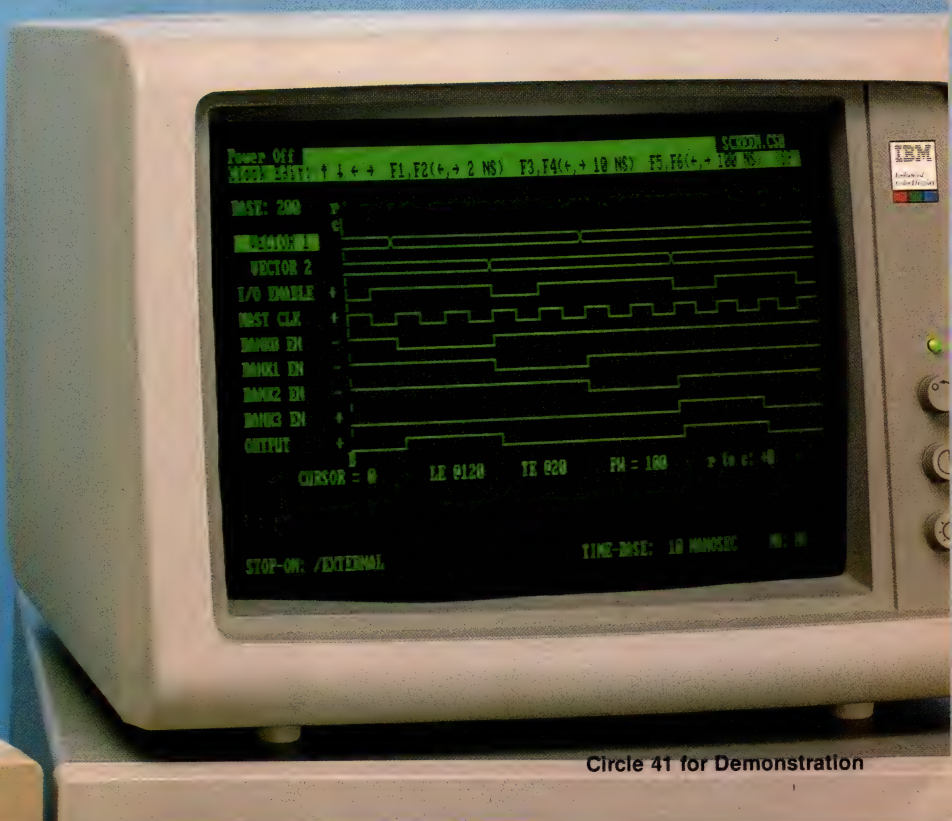

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Circle 2 for Literature

Circle 41 for Demonstration

Simulators that model only signal-delay and timing checks may not be able to simulate transitional ambiguity.

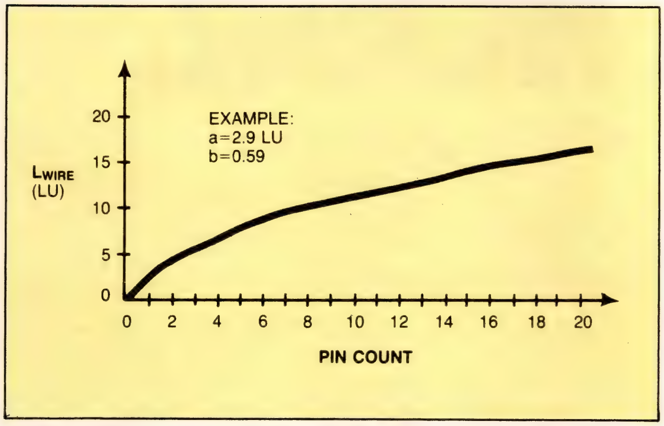

***Fig 9—Statistical wire loading aids simulation** and increases confidence in prelayout simulations. You add estimates of wire loading as a function of fanout (based on completed logic-array designs) to your simulation.*

nets that interconnect the macros have been routed. A simple program extracts the total wire length from the layout data and computes wire loading. Using wire loading, the simulator adjusts the output delays of all macros. The inclusion of wire loading into timing simulation is called back annotation.

Simulation that includes wire and fan-out loading is the last and most comprehensive verification of your design before array fabrication. The accuracy of this simulation depends on the accuracy of the macro models and loading calculations. The actual performance of your array should be in the range defined by the ambiguity window. Typically, this window is within ±10% of the center value of the predicted performance.

If you are designing a high-performance circuit, however, you may need accurate timing simulation before the layout stage. Back annotation is impossible before layout, but a method called front annotation is possible during the design process and can increase the accuracy of your timing simulations. Front annotation attaches statistical loading to each node that approximates the eventual physical loading. The statistical model estimates wire loading as a function of a net's fan-out.

Different approaches are available to estimate wire loading. The simplest method assumes a fixed additional delay for every macro—for instance, 1 nsec. However, statistical analysis of completed logic-array designs reveals that you can attach a more meaningful value of wire load to a macro.

Intuitively, nets with higher fan-out have more interconnect wiring, and therefore more wiring load, than those with low fan-out. A simple statistical analysis of previous logic arrays gives reasonable approximations to the actual wire delays that you can expect in your design.

Statistically, the wire load L_{WIRE} is a monotonically increasing function of the fan-out (also called pin count) of a particular net. The load increase as a function of pin-count increase becomes less significant at higher pin counts. The additional wire load incurred going from a fan-out of 6 to 7 pins is less than that from 1 to 2 pins: With larger pin counts, you have more opportunities to tap into an existing net, so additional pins don't require as much additional metal. Empirically, the statistical wire load follows an exponential law:

$$L_{WIRE}=a(FO)^b,$$

where FO is the fan-out of the net and where a and b are parameters representing the statistical dependence for a particular array type. Variable a is the load associated with fan-out equal to 1; b is an exponent typically less than 1. **Fig 9** shows a typical statistical load dependence on pin count. These statistical load curves are tailored to the particular chip size and even to the circuit density of the chip.

Although front-annotation data comes from actual logic-array designs, it reflects statistical averages. Your routed nets may deviate considerably from front-annotation averages; standard deviations of 50% from the mean aren't unusual. However, you can assume that signal paths with many stages of logic will demonstrate delays close to those predicted using front annotation because the individual net delay deviations tend to average out. In any case, you should always verify a front-annotated simulation after layout using actual back-annotation data.

Average net length used in front annotation may result in wire delays too long for a critical path specification. If your critical signal path is too slow during a simulation that uses front-annotation data, you can resimulate using an approach called selective front annotation. In this type of simulation, you assign a maximum allowable delay to the critical signal path; during layout, you make certain that the actual wire length introduces a delay less than this maximum delay.

By assigning a maximum (or minimum or both) allowed delay, you introduce two conditions. First, the timing simulator uses the assigned delays instead of the front-annotation delays in signal paths. Thus, it makes firm assumptions about the wire load of certain nets. If

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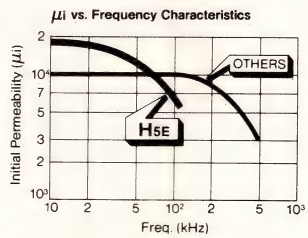

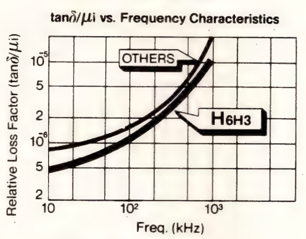

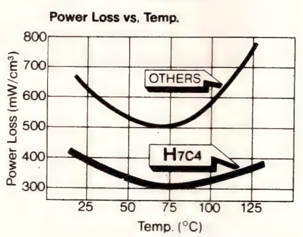

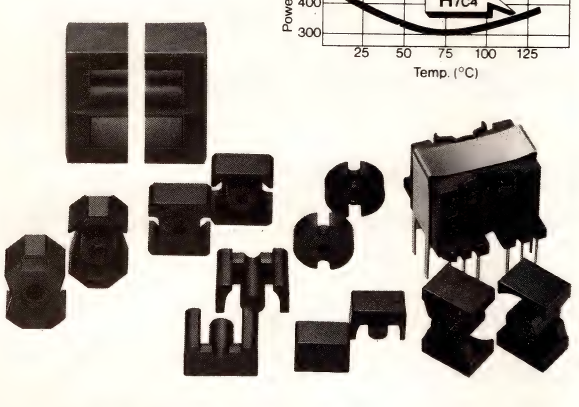

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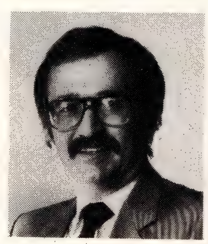
you assign a delay to an entire path, the simulator distributes the delay evenly over the individual nets in the path. The simulator checks for reasonable path delays—ie, it rejects very short wire delays.

The second condition of selective front annotation requires that your logic-array layout system accommodate the initial delay assumption. It places macros connected to critical nets preferentially with the condition that the resulting wiring delay is below the maximum assigned delay. If the assigned delay covers an entire signal path, you can make tradeoffs between the individual net delays of that path. If the layout system can't create nets short enough to exhibit assigned delays, you must manually place the macros. After completing placement, the router attempts to produce interconnect routing with the assigned delay. As is the case with the placement step, you have to intervene manually if assigned delays don't result.

Selective front annotation gives you better control over the dynamics of a logic design than front annotation, thus making prototype performance more predictable. Selective front annotation is particularly applicable to CMOS because of the technology's sensitivity to loading delays. And, it simplifies the interaction between you and the logic-array vendor; you can quantify performance assumptions made during logic design without getting involved in the layout process. **EDN**

Author's biography



Michael Franz is in charge of advanced development at Applied Micro Circuits Corp in San Diego, CA. He performs research and development in the areas of testability, logic simulation, fault grading, and modeling. He holds a Diplom Ingenieur degree from the Technical University in Munich, West Germany, and he received MS and PhD degrees in engineering from the University of Wisconsin at Madison. Michael enjoys sailing and playing the piano.

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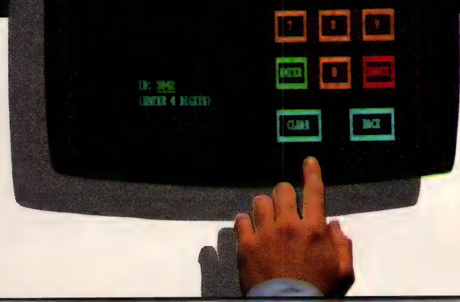

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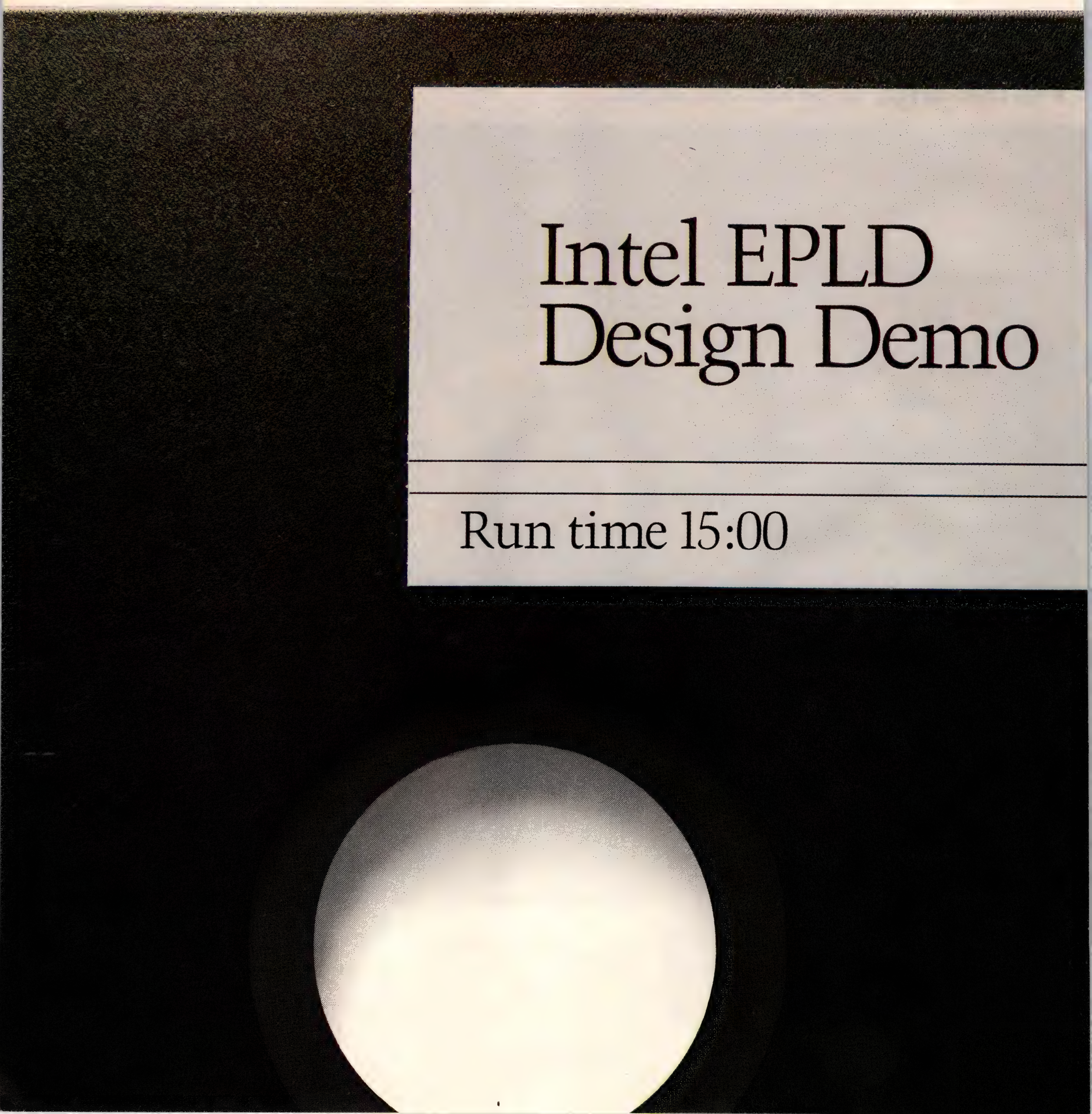

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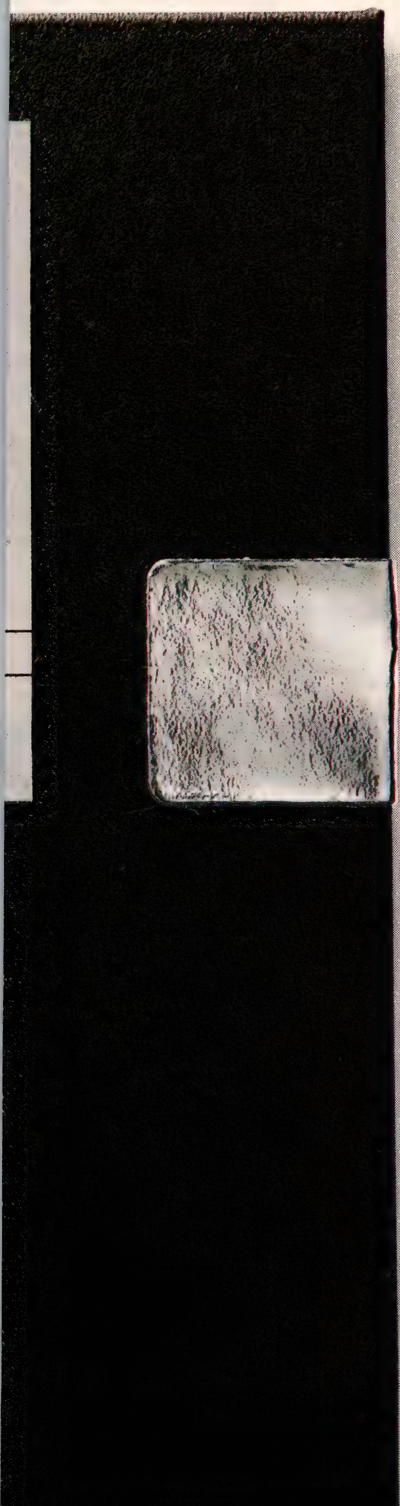

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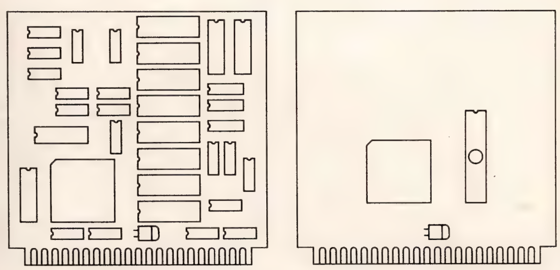

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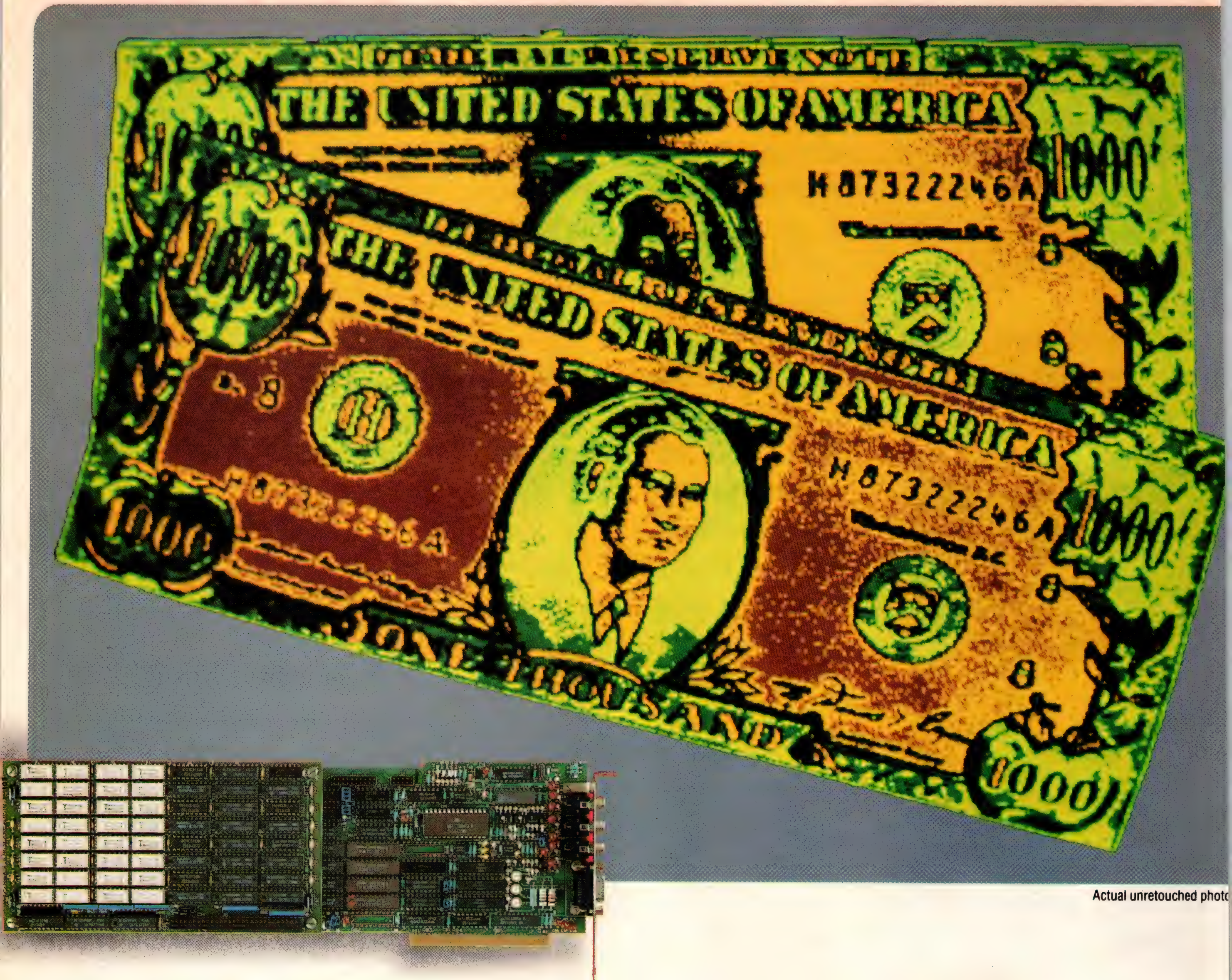

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Semicustom IC offers new possibilities for software protection

Current copy-protection schemes, whether software or hardware based, are not proof against the determined pirate. A semicustom IC allows you to encrypt not only data and instruction words, but also the memory addresses from which instructions are fetched, thereby safeguarding the decryption routines.

David P Lautzenheiser, *Xilinx Inc*

Two advances in technology together offer a potentially dramatic improvement in software security—that is, the prevention of illegal copying. First, the development of "trapdoor" algorithms and random-keyed schemes, which can be implemented in hardware or software, has improved the security of data encryption. More recent has been the development of a logic device that allows you to integrate these sophisticated security schemes into your system hardware.

Most copy-protection schemes are insecure because they rely heavily on the identification of some unique (and constant) characteristic for execution. Software-based schemes typically search for an identifying software fingerprint on the distribution disk—a keyword placed on a track not normally accessible to the system, a physical pinhole in the disk, or some other more complex identifier. Software fingerprints are difficult to write onto the disk and may necessitate the use of special hardware or software.

Hardware-based schemes, on the other hand, contain the identifier in an external physical device that's inserted between the keyboard and the console I/O port or that's attached to some other I/O port. Once loaded into memory from the disk, the protected software periodically interrogates the medium or the external device in some manner; as long as the software detects the presence of the identifier, execution of the program continues.

In either case, security is inadequate because the protection routines that interrogate the identifier are present in the executable memory image of the program. Thus, an ingenious pirate using good debugging/disassembly tools and having plenty of time can identify and bypass the protection routines themselves, as well as each call to them. To guarantee security, you need a method of protection that renders the software unexecutable by the processor unless the protecting mechanism is in place, and that also hides the security routines themselves.

Follow the rules of cryptography

Data encryption by itself is not enough. Unless you take special precautions, the situation will arise when a clear (executable) image of all or part of the program resides in memory and can be dumped to a printer or disk file for disassembly and analysis while the encrypted version, with the bytes in the same order, can likewise be dumped from the distribution disk. This

With current schemes, a determined pirate can identify the security routines and remove all calls to them.

situation violates one of the basic rules of cryptography: You should *never* allow a potential code breaker access to both the encrypted and clear versions of a message.

New protection schemes, based on a logic device (called a Logic Cell Array, or LCA) integrated into the computer system that's to run the protected software, are capable of far more sophistication than schemes based on fixed logic. The high logic density offered by CMOS technology allows the LCA to perform simple readback of a special key sequence—the type of function currently used by most conventional protection schemes—as well as hardware encryption of the data, state-sequence tracking for self-modification of the programming, and other intricate schemes.

Architecturally, the LCA is nearly as flexible as a gate array; moreover, you can reprogram it at any time by means of programming data stored in the device's CMOS static RAM. By means of its program-lock and readback-lock features, you can program the internal gate connections once and then deny any attempt to change or even read the programming data. More important for security applications is the fact that, while still denying any attempt to read the programming data, you can make an applications program modify different sections of the internal data to enable, disable, or dynamically change the encryption scheme.

You can safeguard the protection algorithms themselves by molding the backup battery into the LCA housing; then, any attempt to tamper with the device will break the battery connections and destroy the stored programming data. The power-down current of the LCA is so low that a lithium battery is capable of preserving the programming data throughout the battery's shelf life, which spans decades.

The main difference between current security schemes **(Fig 1a)** and those based on the LCA **(Fig 1b)** is that operation of the LCA is intimately linked to, and is a function of, the interaction between the protected software and the hardware executing that software. The complexity of the interaction between the software, the hardware, and the LCA determines the degree of security you can achieve.

Implementing a protection scheme of the type shown in **Fig 1b** involves both the software developer and the manufacturer of the hardware on which the software is to run. The hardware manufacturer provides the protection device and programming, the interface between the device and other portions of the system, as well as the necessary information and personalization data for the scheme being implemented. Once the basic hardware capability is available, the software vendor is in control of the remainder of the process.

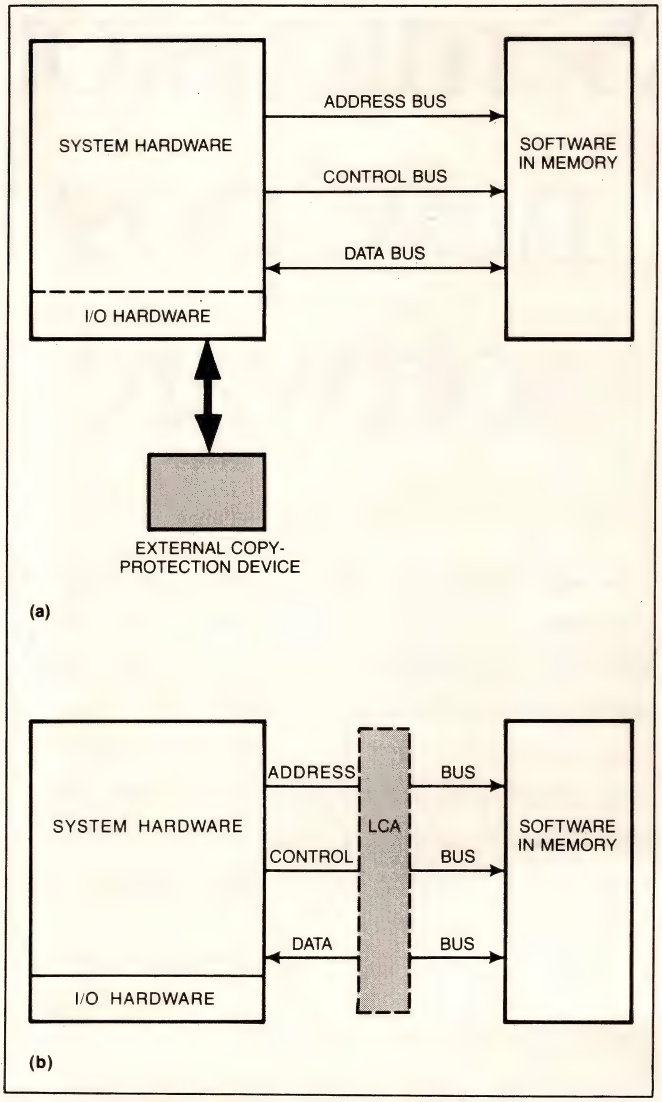

Fig 1—Current hardware protection methods (a) aren't secure *because calls to the interrogation routines are identifiable in main memory. Schemes using the LCA* ***(b)*** *can encrypt addresses as well as data and can disguise the processor cycles that trigger scrambling/unscrambling.*

Personalization of a software system to fit a particular hardware configuration is based upon a serial-number hashing algorithm provided by the hardware vendor. The software developer and the hardware vendor together decide which type of protection is needed. The LCA can provide three types of protection, which you can use singly or in combination: file encryption, address scrambling, and data scrambling.

File encryption provides the executable code files in a

form that's not directly executable by the processor. The disk contains execution files in encrypted form, together with a small decrypting loader. When you call for execution of the software, the operating system brings the decrypting loader into memory and executes it. The loader, in turn, fetches the remainder of the software, passing it through the hardware decryption processor to obtain an executable memory image of the protected software.

In an IBM PC environment, for example, the LCA and its supporting logic can be mounted on a small plug-in card **(Fig 2)**. Decryption, in this case, is activated by detection of a restart triggered by a state machine that's controlled from I/O-cycle-detection logic. The state machine allows the software to restart the decryption process at selected times; alternatively, you can require a system reset in order to perform decryption restart.

You can implement either of two decryption methods in the LCA. The first **(Fig 3a)** uses a long linear-feedback shift register (LFSR) to create a long binary polynomial; selected feedback points determine the active terms of the polynomial. Software vendors provide their products encrypted with the same polynomial feedback terms, and processing the encrypted data through the LFSR produces the original, executable instructions in memory.

The second method **(Fig 3b)** uses a similar technique except that the data is processed in byte-parallel fashion, the polynomial being determined by the interbyte feedback paths. This method has the advantage of needing fewer clock cycles to pass bytes through the processing registers. Nonetheless, the only truly significant difference between the two methods involves the time it takes for the first byte to traverse the registers; while the pipeline is full, bytes emerge at the same intervals from both serial and parallel versions.

However, no matter how good the encryption technique, file encryption still suffers from the disadvantage mentioned earlier: Clear and encrypted versions of the program are available simultaneously, and the bytes are in the same order in both. Thus, a computer-aided expert cryptographer might, in time, be able to discover the encryption algorithms and keywords—even though encryption of 16-bit computer words, rather than of individual bytes, would make the task more difficult.

The LCA's address-scrambling capability overcomes the disadvantage of having both code and clear versions of the program with the bytes in the same order.

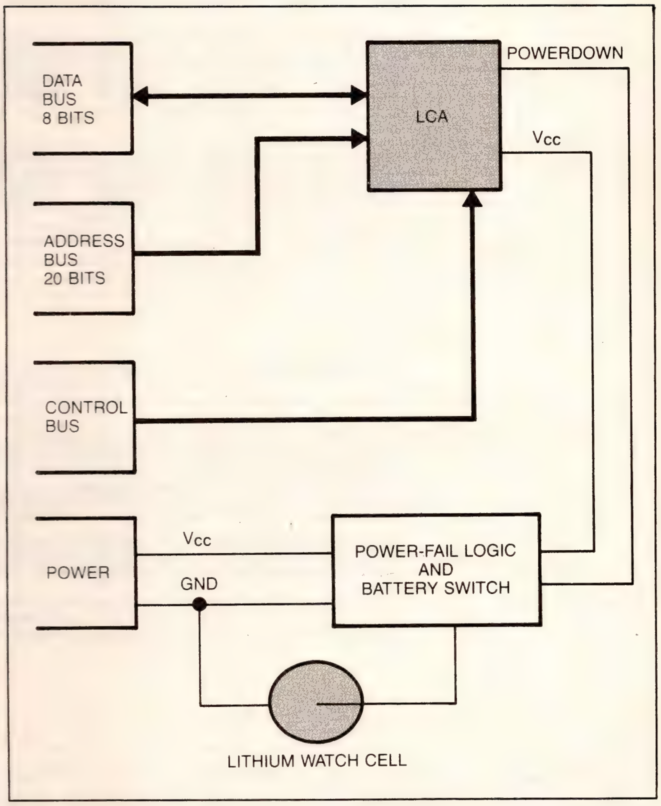

*Fig 2—**In an IBM PC environment,** you can encapsulate the LCA and its backup battery and mount them, together with the CPU chip, on a small card that plugs into the processor socket. The LCA then has complete control of the bus lines.*

However, this scheme requires much tighter coupling between the execution hardware and the protection hardware **(Fig 4)**, and it can't be implemented on a plug-in auxiliary card.

During normal operation, the LCA is transparent to the use of the memory, but when the protected software begins operating, it also starts operation of the protection hardware. The function of the LCA is to scramble the memory addresses from which the μP fetches bytes for execution in a manner known to the software developer. Even if the data itself is not encrypted, normal debugging and disassembly software won't work because the sequence of bytes in the memory image bears no obvious relation to the sequence in which they are actually fetched for execution. A branch op code and its target address bytes might be separated in memory by many hundreds of locations so that a disassembler would become hopelessly confused.

You can also apply the technique of execution-dependent scrambling to data bits rather than address bits. This method is inherently less effective than address

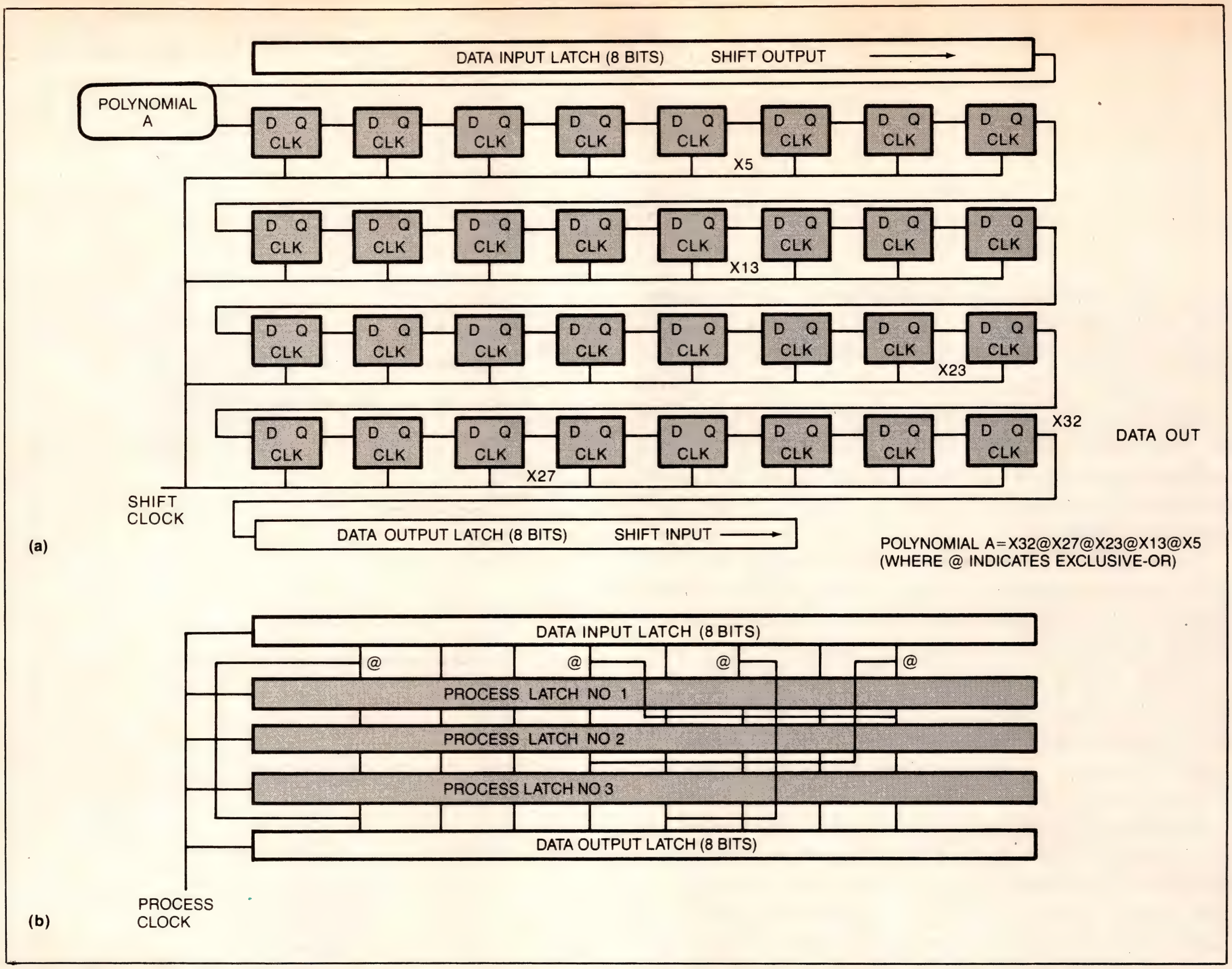

Fig 3—You can program part of the LCA to act *as a long shift register* ***(a)*** *to encrypt or decrypt data, or you can organize the LCA as a set of parallel processing registers* ***(b)****. The pattern of exclusive-OR connections determines the encoding/decoding polynomial.*

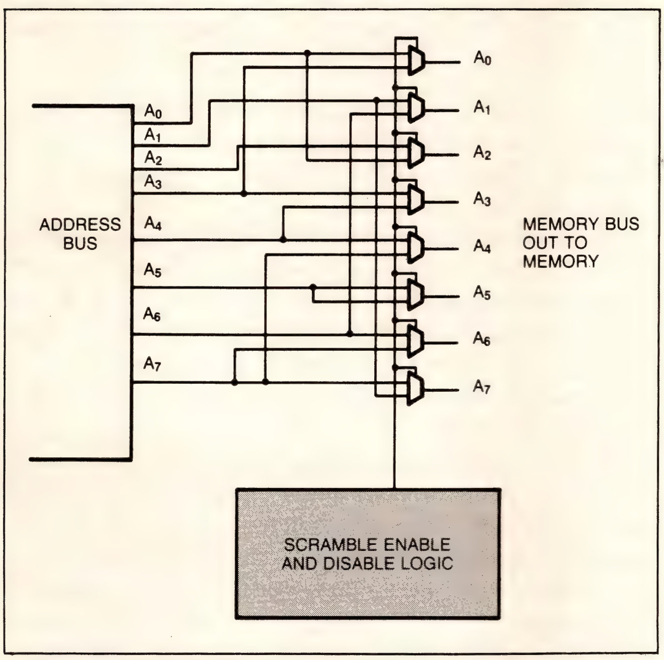

Fig 4—You can improve security by programming the LCA *to scramble the addresses from which the processor fetches instructions for execution. The scrambling separates op codes from their arguments and makes the program much more difficult to disassemble.*

scrambling, however, partly because the data word may have fewer bits (and therefore fewer permutations) than the address word, but also because the scrambling doesn't disrupt the sequence in which bytes are fetched. Thus, the primary level of security depends on the degree of sophistication built into the scramble-enabling and -disabling logic.

Nevertheless, this scheme, too, puts blocks in the path of software debugging tools. If the debugger initiates a data write while scrambling is taking place, the data written will be incorrect if read back without scrambling. The reverse is also true; data written while scrambling is disabled will be read incorrectly while scrambling is taking place.

One difficulty implementing an address- or data-scrambling scheme is related to the unpredictable interactions between the software and the keyboard input, disk I/O, and interrupt servicing. These asynchronous events disrupt the normal execution flow and potentially interfere with the scrambling operation. One way of eliminating these difficulties is to disable interrupts while executing the scrambled portion of the software. Another alternative is to trigger execution of the scrambled portions of the software by means of a

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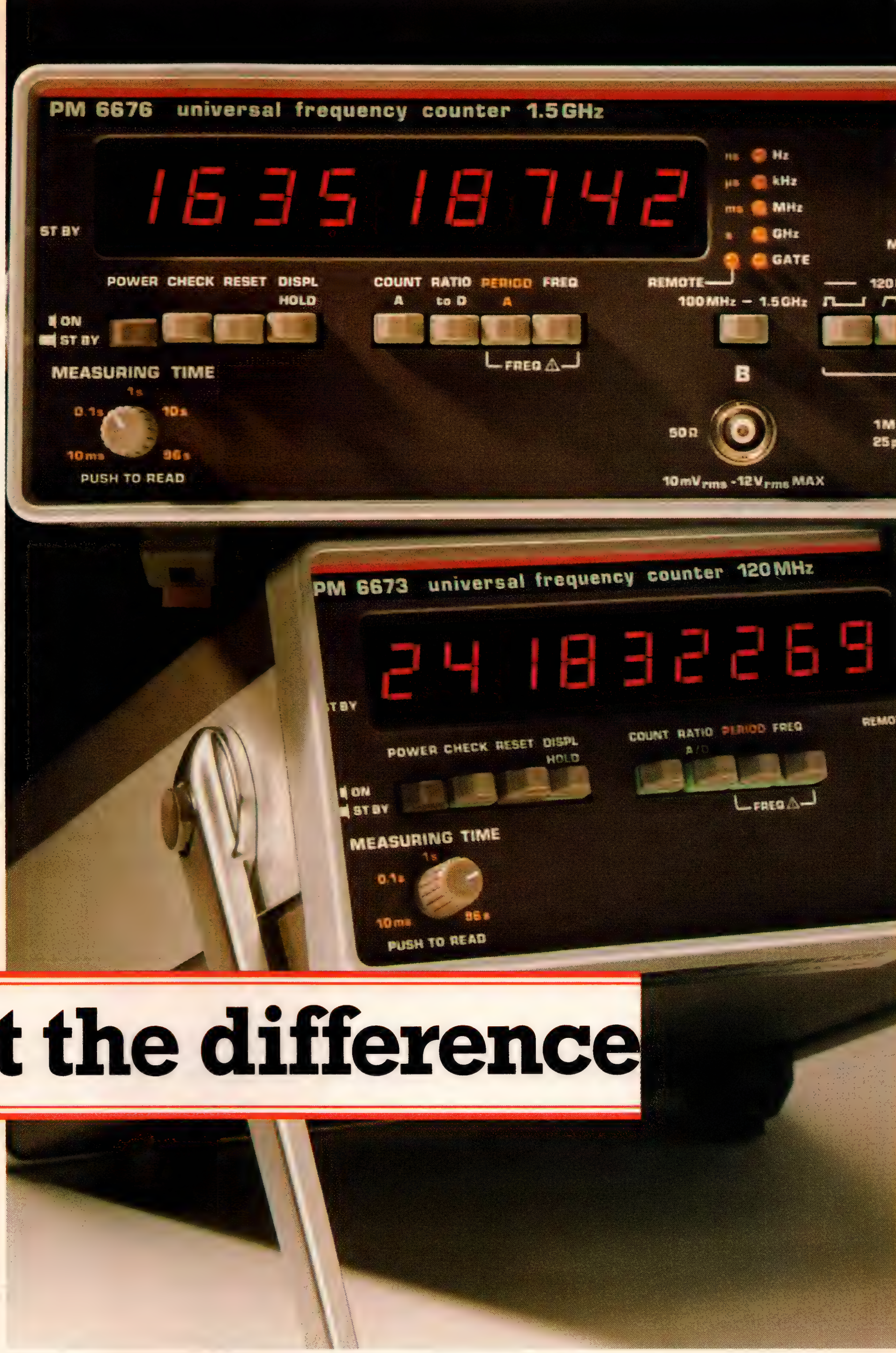

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File encryption alone is insecure because a clear version (in memory) and the encrypted version (on the disk) are simultaneously available to a pirate.

hardware or software interrupt; this technique makes the use of software debugging tools even more difficult.

For example, to enable or disable scrambling, the address decode logic in **Fig 5** determines a range of addresses that can potentially activate the scrambler. When the cycle-detect logic senses the selected type of cycle (in this case a memory write), the end of that cycle sets the enable flip-flop, disables the enable-detection logic, and enables the disable-detection logic. While the enable flip-flop remains set, the addresses will be scrambled according to the interconnect pattern routed to each of the address-bit multiplexers. The type of cycle that stops the scrambling process need not be the same as that which starts the scrambling; the disable-detection logic might, for instance, sense an I/O read cycle performed at address 94H to stop the scrambling.

You can make life more difficult for a pirate by varying this basic address-scrambling scheme in any of three ways. First, you can vary the number of address bits transposed from two bits to all the address bits. Second, you can vary the type of cycle sensed by either the enable or the disable decode logic, or both. Third, you can interpose a delay of some number of clock or processor cycles between the sensing of an enable/disable cycle and the starting/stopping of the scrambling. This procedure makes it more difficult to identify the cycle that is acting as the trigger, particularly if you vary the delay dynamically.

Software security needs cooperation

For the most effective use of the LCA, the device should be tightly coupled to the hardware on which the software is to run; such an implementation requires close cooperation between the software developer, the manufacturer of the execution hardware, and the LCA manufacturer. Whether or not such cooperation is possible depends largely on the willingness of users to accept any restrictions that the installation of LCAs might impose on changes and upgrades to their hardware.

It's worth noting, however, that LCA-based protection schemes don't prevent users from making legitimate backup copies at any time; the copies can still be run only on the specific machine or machines for which the software has been licensed. It's the restrictions imposed by many current schemes in this respect—not to mention the loss of valuable data that has resulted from bugs in some schemes—that make copy protection detestable to most individual users and to many large corporations. **EDN**

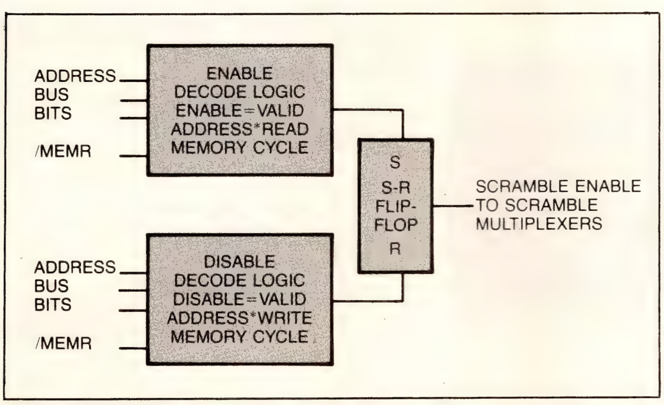
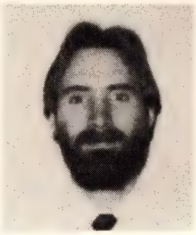


Fig 5—You don't have to scramble all of your program. *You can start and stop scrambling by detecting a particular kind of processor cycle within a range of memory addresses; the cycle that stops scrambling need not be of the same type as the cycle that starts it.*

Author's biography



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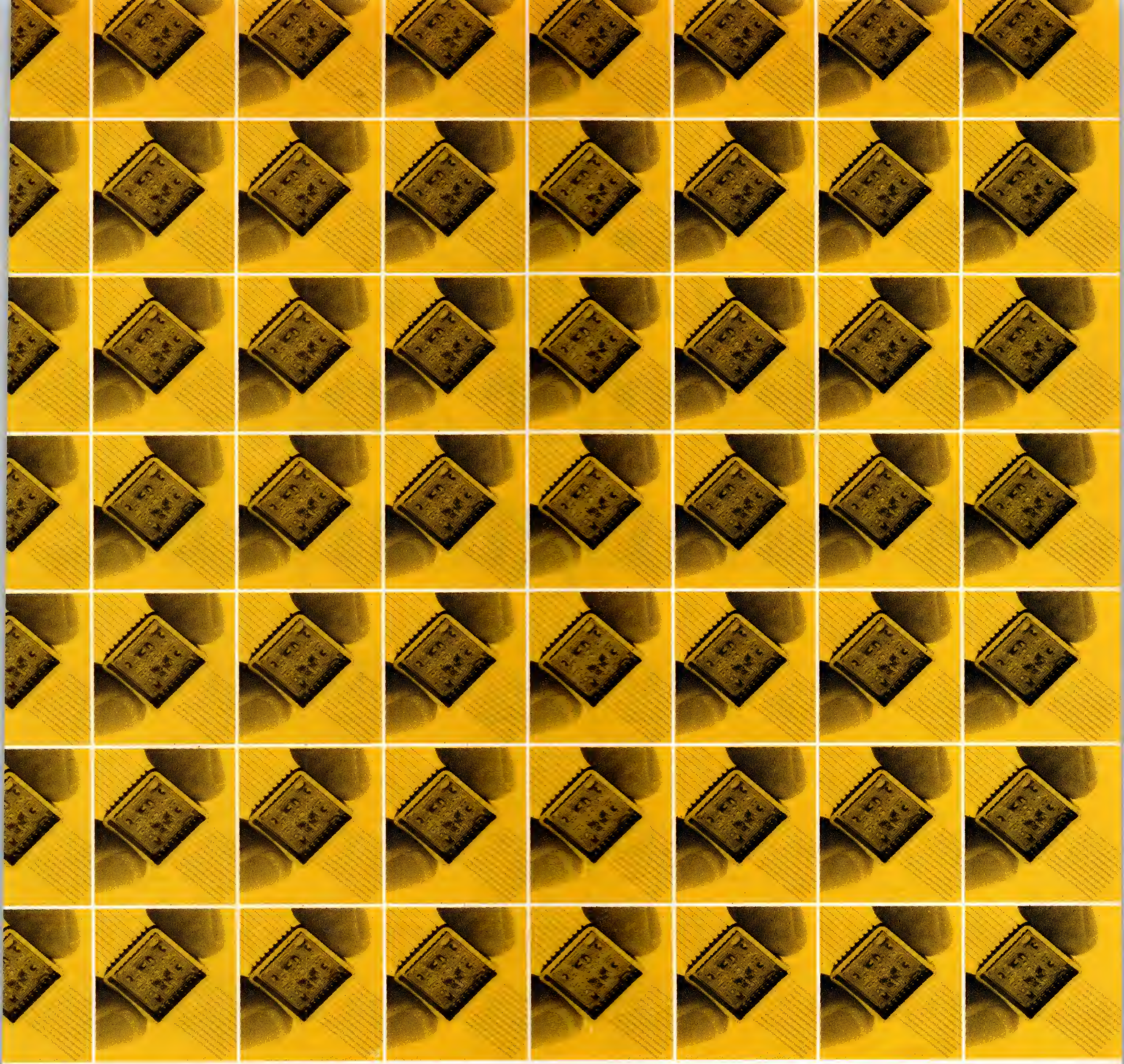

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Design current-mode switching supply on analog workstation

You can easily design a current-mode switching power supply that exhibits very stable output characteristics. Instead of using advanced design theories or linearizing techniques based on approximations, you can simulate your supply's operation on an analog CAE workstation, using straightforward techniques.

Norman C Walker, *Walker Electronics*, and
Martin G Walker, *Analog Design Tools*

By using a simple approach, you can easily create a current-mode switching power supply on an analog workstation. After completing your design, you can use the program's analysis functions to see how component tolerances will affect the transient performance of your regulator.

Fig 1a illustrates the use of the current-mode-control technique in a fixed-frequency, nonisolated buck converter with peak-current sensing. To understand the operation of the current-mode controller, first examine the inner loop, which comprises the latch, switch, sense amplifier, and comparator. At the leading edge of the clock, the latch sets and turns on the switch, increasing the current flowing through the inductor. When the

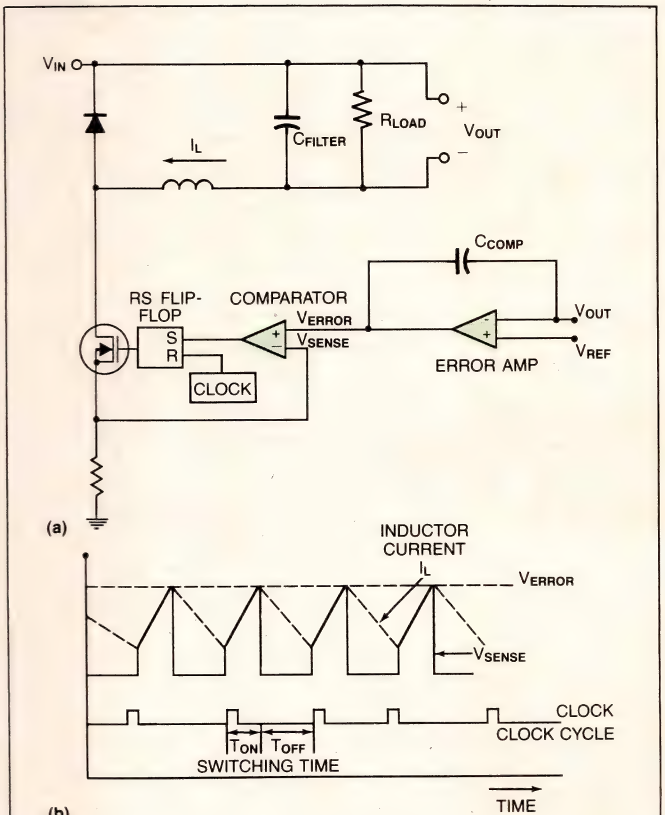


Fig 1—By closing a loop around the filter inductor, *the current-mode-control approach **(a)** provides more stability than does a pulse-width-modulation design. As the waveforms **(b)** illustrate, the error voltage directly controls the peak inductor current.*

To efficiently simulate the circuit's steady-state operating point, you must first estimate the state of the energy-storage elements having the largest time constants.

sense voltage (which is proportional to the switch current) exceeds the output of the error amplifier, the latch resets.

The latch reset turns off the switch, and the inductor current starts to decrease. **Fig 1b** shows this switching sequence. The error voltage directly controls the peak inductor current, which is directly related to the average current. When you analyze the complete circuit, therefore, you can replace this inner loop with a voltage-controlled current source whose gain equals g_m.

The loop gain of the entire circuit is

$$(A_{ERROR})\,(g_m)\,(Z_{OUT})\left(\frac{1}{K}\right), \tag{1}$$

where A_{ERROR} is the gain of the error amplifier, g_m is the voltage-to-current gain of the inner loop, Z_{OUT} is the parallel impedance of the filter capacitor and load, and K is the voltage-divider ratio of the output-voltage sense circuit. At frequencies greater than a few Hertz, the loop gain is

$$\left(\frac{1}{s\,C_{COMP}}\right)(g_M)\left(\frac{1}{s\,C_{FIL}}\right)\left(\frac{1}{K}\right). \tag{2}$$

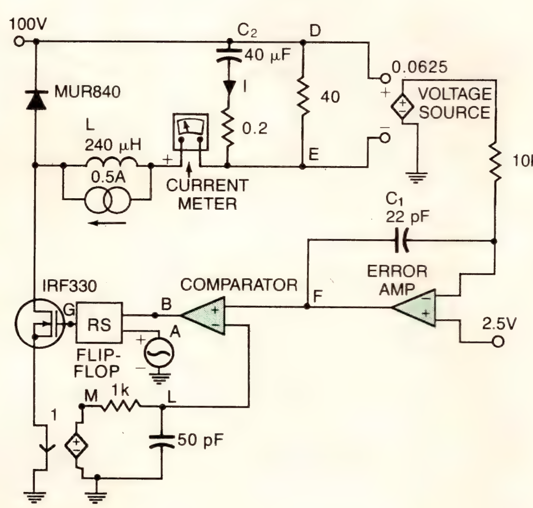


Fig 2—A key component in this current-mode converter *is the Unitrode 1842 controller IC, which contains an error amplifier, comparator, and a latch.*

To find the circuit's output voltage and inductor-current ripple, as well as the switch's on-time, you can use the following equations **(Ref 1)**:

$$V_{OUT} = \left(I_C - \frac{\Delta I}{2}\right) R_L, \tag{3}$$

$$\Delta I = T_{ON}\,\frac{(V_{IN} - V_{OUT})}{L}, \text{ and} \tag{4}$$

$$T_{ON} = \frac{V_{OUT}}{V_{IN}}\,(T), \tag{5}$$

where I_C is the control signal, ΔI is the inductor-current ripple, T_{ON} is the switch's on-time, and T is the clock period.

Analyzing power-supply performance

Although you can predict the performance of current-mode power supplies by using certain linearizing or averaging techniques based on approximations **(Refs 2 and 3)**, these methods have a major drawback: As the speed of transients approaches the loop-response time, your approximations become less exact. The current-mode-control technique, however, is most useful in the high frequency ranges, so such approximations will usually pose problems in current-mode power-supply designs.

You don't need to make such approximations when you use the Analog Workbench program (see **box**, "A look at an analog CAE tool"). To obtain a detailed and accurate prediction of your circuit's performance, the program analyzes the circuit on a point-by-point basis for several cycles of the switching frequency. Because of the fast response of the current-mode supply, 10 switching-frequency cycles are enough for the output to reach steady-state conditions. With the exception of the statistical analyses, each of these analyses takes about 10 to 15 minutes.

Establishing the design goals

Although the following sections illustrate the design and analysis procedures for a buck converter, the design methodology applies to current-mode converters in general. For this sample circuit, assume that your goal is to design a supply that delivers 40V at 2A, switches at 100 kHz, operates from a 100V input, and has an 80-µsec loop response.

The first step in your design procedure is to specify

A look at an analog CAE tool

The current-mode switching power supply described in this article was simulated on the Analog Workbench CAE program from Analog Design Tools (Menlo Park, CA). The program can reduce the time-consuming tasks associated with analog-circuit design by allowing you to simulate the entire design process, from schematic drawing through breadboarding, testing, and performance analysis.

The Analog Workbench is available for Sun, Apollo, and HP 9000 Series 300 workstations, as well as for the IBM PC/AT. Spice Plus, Analog Workbench's analysis program, is based on an enhanced version of the University of California at Berkeley's Spice 3.

your circuit's components and select values for R_T and C_T. In **Fig 2,** for instance, the off-line current-mode controller IC is a Unitrode UC1842. The switch is an IRF330 HEXFET, and the freewheeling diode is a fast-recovery MUR840. The CAE program provides models of these parts: The program's UC1842 model, for example, consists of an error amplifier, a comparator, and an output latch (including buffers).

The program's function generator, which is programmed to provide a 10-μsec clock pulse and a 1-μsec dead time, replaces the clock section of the controller. Although this simplification has no effect on the accuracy of the simulation, it will reduce the analysis time.

You then enter the circuit directly on the workstation's screen. In **Fig 2,** an 0.2Ω resistor simulates the series impedance of the 40-μF filter capacitor. The 1-kΩ/50-pF lowpass filter serves to reduce the gate-switching transients on the current-sense waveform **(Ref 4).**

Because the circuit settles in about three time constants, you'll require a bandwidth of 12 to 15 kHz in order to obtain an 80-μsec loop response. When you set ω equal to 2π(15 kHz), you can use **Eq 2** to solve for C_{COMP}. The calculation yields a value of about 25 pF, but a standard 22-pF capacitor will suffice.

To effectively simulate the circuit's steady-state operating point, you must first estimate the state of the energy-storage elements that have the largest time constants. In the circuit in **Fig 2,** these elements are the filter inductor, the filter capacitor, and the compensation capacitor. The remaining time constants in the circuit are very short, so they'll relax to the correct operating points soon after the simulation begins.

It's a good idea to calculate the state of the circuit just before the clock turns the switching transistor on. Using **Eq 4** and setting the load at 40Ω, you obtain an average inductor current of 1A:

$$\Delta I = \left(\frac{60}{240}\right)(0.4)\,10^{-5} = 1A. \qquad \textbf{(6)}$$

The initial inductor current, therefore, is 0.5A. The switch transistor turns off at a 1.5A current level, so the error amplifier's output equals 1.5V. The error amplifier's input is the same as the reference voltage (2.5V), and the voltage across the filter capacitor is 40V. After you enter these initial conditions, the program will display the schematic shown in **Fig 3.**

It's not necessary to make a precise calculation of the initial conditions; if you've made any errors, the circuit will simply require a few extra clock cycles to reach steady state. The program performs the circuit analysis as soon as you've set the initial conditions; **Fig 4a** shows the circuit's output voltage, control voltage, and inductor current.

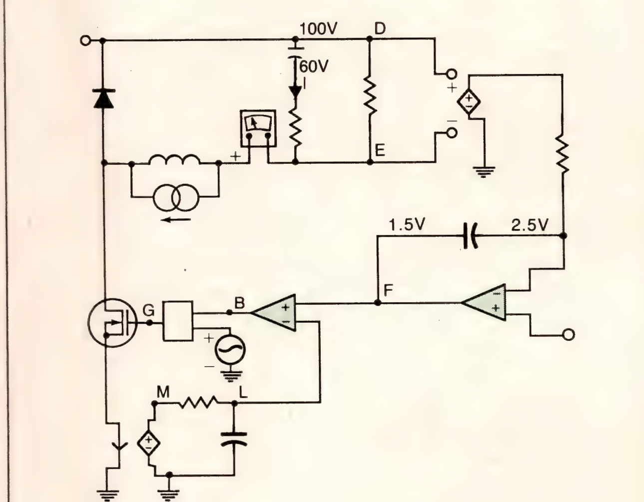


Fig 3—After you supply the initial conditions *to the Analog Workbench program, the converter circuit will appear on the workstation monitor as shown here. The paralleled current source models the initial inductor current.*

A current-mode-control scheme exhibits open-loop instability for duty cycles greater than 50% **(Ref 3)**; even for duty cycles less than 50%, the circuit exhibits a peak response at half the switching frequency **(Ref 4)**. The circuit's instability is even more pronounced under transient load conditions.

Fig 4b shows how the circuit performs in response to a 1A load switched onto the output 3 μsec after the analysis begins. As the output-voltage waveform shows, the circuit experiences considerable ringing, which extends well beyond 150 μsec. Note that this serious problem shows up in the power-supply circuit even for a 40% duty cycle—a percentage at which the circuit is theoretically stable.

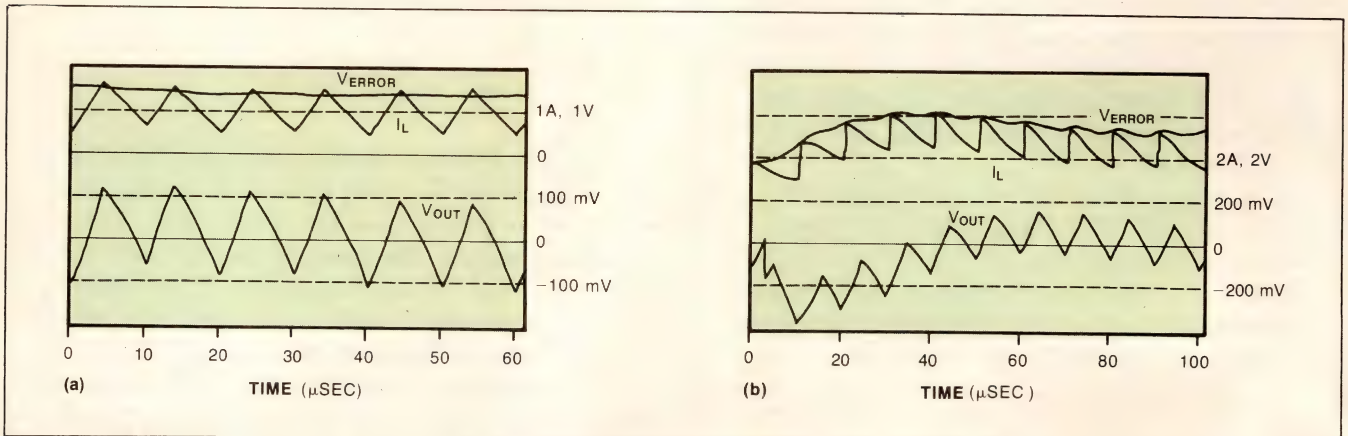


Fig 4—Simulation of the circuit *shown in* ***Fig 3*** *results in the waveforms shown in* ***a*** *when initial conditions are set. In response to a 1A load applied 3 μsec after the analysis begins, the simulation yields the waveforms shown in* ***b.***

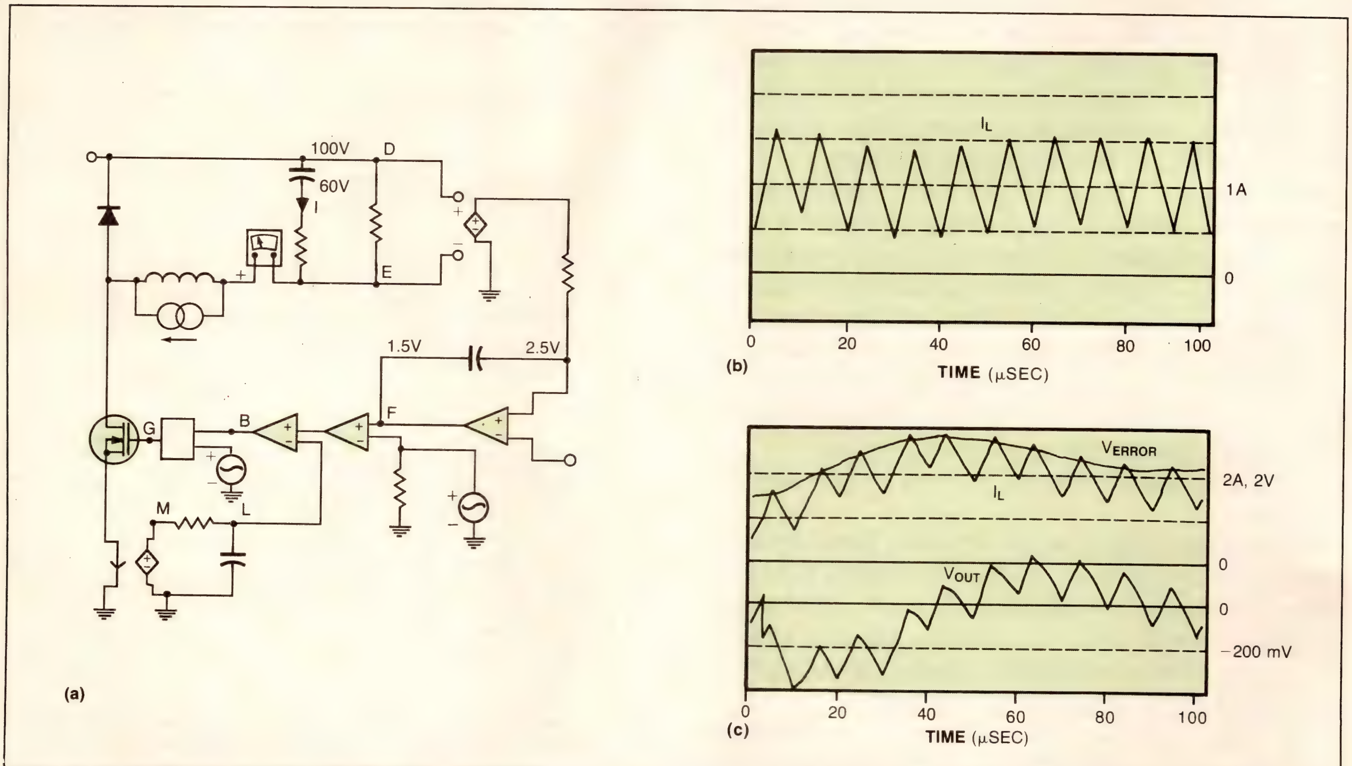


Fig 5—To provide slope compensation, *you need to make some modifications to the basic converter* ***(a).*** *The inductor-current waveform* ***(b)*** *and the transient performance* ***(c)*** *show the modified circuit's operation.*

You don't need to calculate initial conditions precisely; any errors will simply force the circuit to go through a few extra cycles to reach steady state.

To solve this oscillation problem, you can use the slope-compensation technique **(Ref 4).** Using slope compensation, you take a signal whose slope is equal to half the slope of the inductor current when the switch is off, and sum that signal with the error-voltage waveform. To perform this summing task, you must modify the circuit as shown in **Fig 5a**. **Fig 5b** shows the steady-state operation of the modified circuit; this waveform is now symmetrical, which indicates that the circuit's stability is improved.

The waveforms in **Fig 5c** show the circuit's transient response, which is still underdamped. You can solve this problem by placing a 500-kΩ resistor in series with the compensation capacitor. This modification adds a zero to the transfer function at about 15 kHz, thus improving the phase margin by almost 80°. As **Fig 6** demonstrates, this scheme significantly improves the circuit's performance: The circuit now appears to be almost critically damped.

When your design is nearly complete, you'd be wise to use the program to check the stress level of the critical switching components (the diode and the FET) in the circuit **(Fig 7a).** Power dissipation in the FET switch is lower than 6W, which is well within the device's 75W safe operating area.

In addition, you should run a test to ensure that transients caused by overcurrent conditions on the output don't exceed device specifications. You can test for these conditions by switching an 8Ω load into the circuit at the beginning of the analysis. **Fig 7b** shows the peak switch current. You should also run tests to investigate circuit behavior under discontinuous-conduction (light-load) conditions.

Evaluating component-tolerance effects

Your next step is to evaluate the effects of component tolerances on the supply's performance. Filter-inductor and filter-capacitor values are both very difficult to control accurately. Inductor values may vary by as much as 20%, and −20/+80% tolerances are typical for capacitors. You can use some of the CAE program's analysis features to determine how these variations will affect your circuit's performance when it's actually in production.

The values of the filter capacitor, filter inductor, compensation capacitor, and compensation resistor have a direct effect on the loop's transfer function. When your power supplies are actually in production, variations in the values of these components may seriously affect circuit damping.

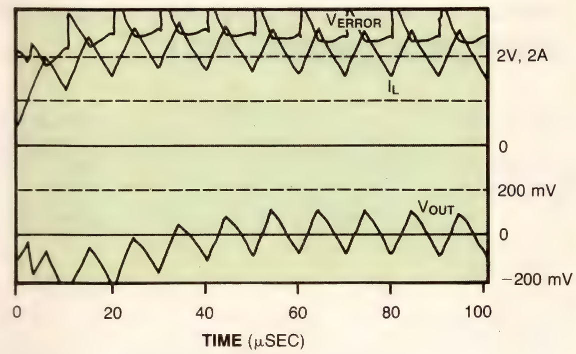


*Fig 6—**You can correct damping problems** by placing a 500-kΩ resistor in series with the compensation capacitor. After you make this simple addition, the waveforms show that the circuit is almost critically damped.*

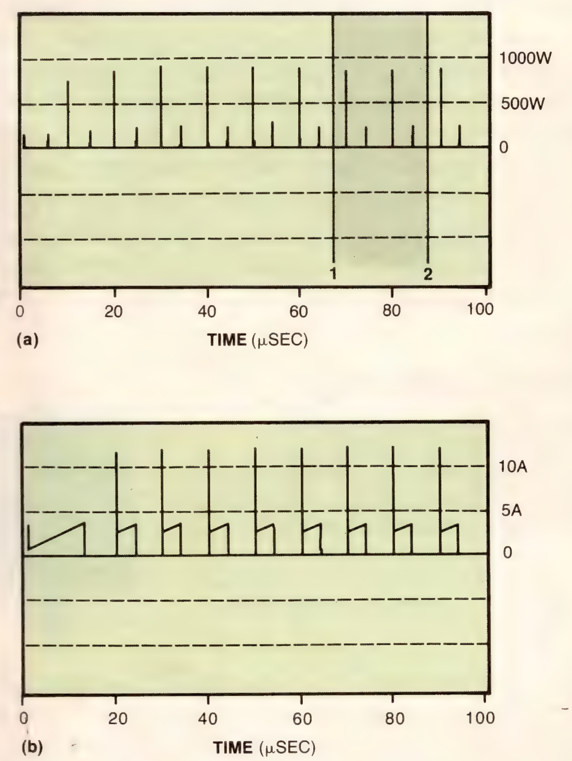


*Fig 7—**A stress-level check** shows that the average power dissipation in the FET switch **(a)** is 5.57W, as determined by averaging the power from marker 1 (set at 67.5 μsec) to marker 2 (87.5 μsec). The waveform in **b** indicates the peak current in the switch in response to an overcurrent condition on the output.*

As your converter design nears completion, it's important to check the stress level of the circuit's critical switching components.

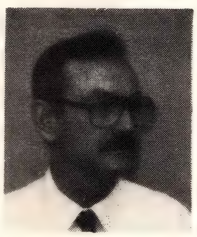
TABLE 1—WORST-CASE ANALYSIS OF COMPONENT SENSITIVITY*

COMPONENT	VALUES			RELATIVE SENSITIVITY
	NOMINAL	MINIMUM	MAXIMUM	
FILTER INDUCTOR L	240 μH	192 μH	288 μH	1.491 mV
FILTER CAPACITOR C_2	40 μF	30 μF	100 μF	407.537 μV
COMPENSATION CAPACITOR C_1	22 pF	24.2 pF	19.8 pF	−261.307 μV

* VALUES SHOWN ARE FOR THE BUCK-CONVERTER CIRCUIT IN FIG 2.

To investigate this possibility, you can use the program to determine which of these components will have the greatest effect on the circuit's overshoot when it responds to the 1A transient. In the sample circuit, the inductor is the most sensitive component **(Table 1)**. However, even in the worst case, the transient will only be 200 mV greater than it would in the nominal case. As a further prediction of the performance of your production-line supplies, you can run a Monte Carlo analysis on the workstation to measure the output ripple for a 2A steady-state load condition. **EDN**

Authors' biographies



Norman C Walker is the owner of Walker Electronics (Villa Park, CA), where he provides circuit-design consulting. He received BSEE and MSEE degrees from the University of California at Berkeley, and he has been awarded four patents. Norm spends his spare time skiing, fishing, and sailing.

Martin G Walker is vice president of advanced development at Analog Design Tools Inc (Menlo Park, CA). A cofounder of the company, he directs a team that evaluates technical opportunities for the firm's Analog Workbench, and he's currently developing additional analysis and simulation tools. Marty has a BSEE degree from MIT and MSEE and PhD degrees from Stanford University. A member of IEEE, he enjoys skiing, opera, and racquetball in his free time.

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Acknowledgment

The authors wish to extend their appreciation to Hal Conklin of Analog Design Tools Inc for his help in the preparation of the diagrams appearing in this article.

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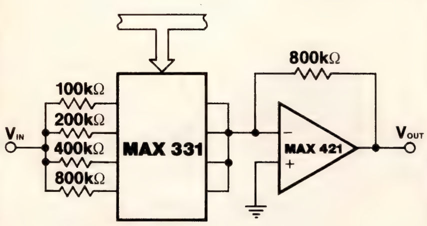

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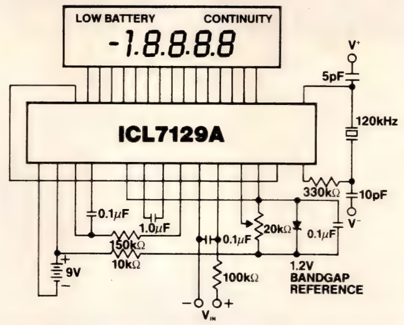

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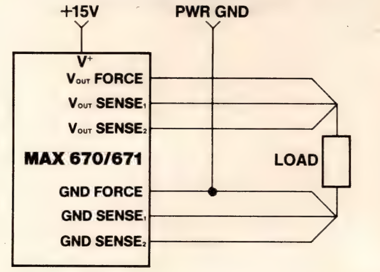

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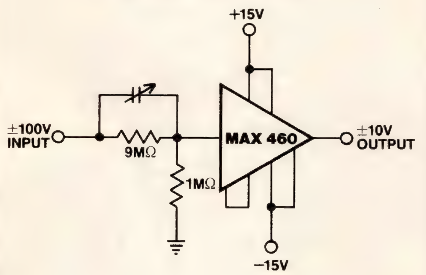

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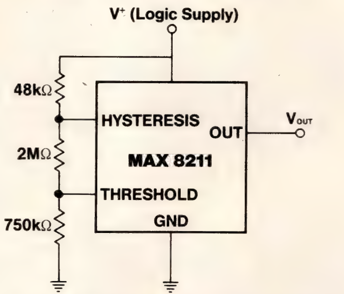

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CIRCLE NO 206

Solve oscillation problems when implementing op-amp power-booster stages

You can increase a low-level op amp's output voltage or current capability (or both) by employing a power-booster stage like the ones discussed in part 1 of this 2-part series. However, the additional phase shift introduced by including such a stage within an amplifier's feedback loop can increase the likelihood of oscillation, unless you judiciously apply frequency-compensation methods.

Jim Williams, *Linear Technology Corp*

To attain greater outputs from monolithic op amps with limited voltage and current capability, you must add a power-gain stage, such as one of those discussed in part 1 (**Ref 1**) of this 2-part series. But a circuit's overall phase shift, frequency response, and dynamic load-handling capabilities are critical when you include such a stage within an op amp's feedback loop. All feedback systems, including operational amplifiers, have gain and phase shift and, therefore, the propensity to oscillate. A booster stage's added gain and phase shift can cause poor ac response or outright oscillation. When applying such a stage, then, you must consider its gain and ac characteristics to ensure that your circuit achieves good dynamic performance.

A large body of complex mathematics is available that describes stability criteria and that can aid you in predicting stability characteristics of feedback amplifiers. The most sophisticated applications require this effort so that your circuits achieve optimum performance.

However, until now, little has appeared which discusses, in practical terms, how to understand and address the issues of compensating feedback amplifiers. Oscillation problems in amplifier/power-booster-stage combinations fall into two broad categories: local oscillations and loop oscillations. Local oscillations can occur in the boost stage, but they shouldn't appear in the IC op amp (which the manufacturer presumably debugged prior to sale). Transistor parasitics, layout, and CRT configurations cause these oscillations.

Usually, local booster-stage oscillations don't cause loop disruption. The major loop continues to function but contains artifacts of the local oscillation. In **Fig 1a** (which appeared as **Fig 8a** in **Ref 1**), the Q_3 and Q_5 and Q_4 and Q_6 pairs have a high gain-bandwidth product. The resistive feedback loops allow the pairs to oscillate in the 50- to 100-MHz region without the 100-pF/200Ω network shunting the dc-feedback resistors.

This network rolls off the transistors' gain-bandwidth product, preventing oscillation. It's worth noting that a ferrite bead in series with the 2-kΩ resistor will give similar results. In this case, the bead would raise the inductance of the wire, attenuating high frequencies.

Fig 1b depicts how the circuit would respond to a bipolar square-wave input if the local high-frequency,

If an output stage resides in an amplifier's feedback path, you must be concerned with the feedback loop's stability.

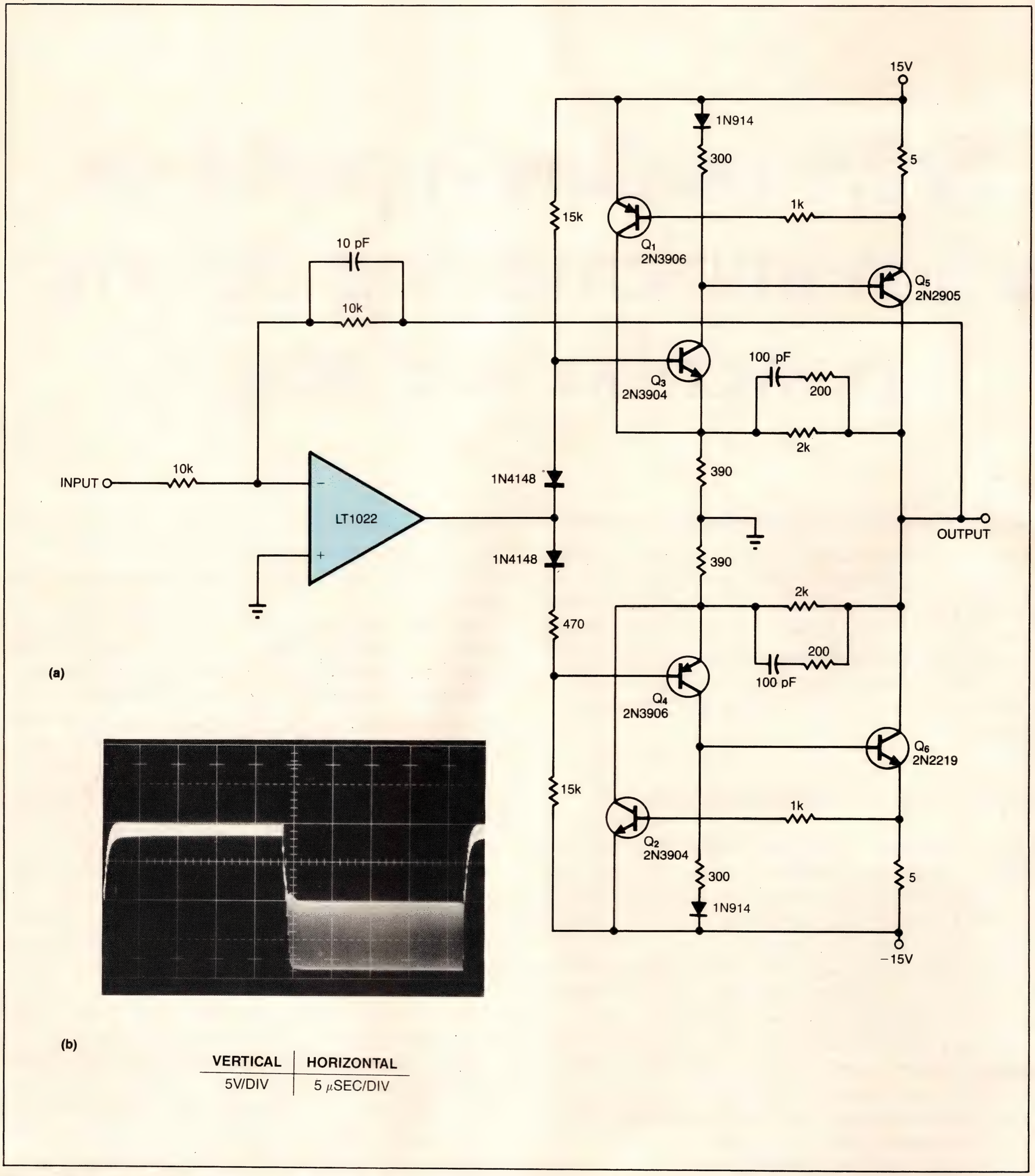


***Fig 1—Removing the compensation networks** of this circuit **(a)** and applying a bipolar-square-wave input results in high-frequency oscillation **(b)**, which is typical of locally caused disturbances.*

RC compensation networks were removed. The resultant high-frequency oscillation is typical of locally caused disturbances. Note that the major loop is functional, but the local oscillation corrupts the waveform.

Evaluate devices

You can help eliminate such local oscillations by selecting the proper device. Avoid high-f_T transistors unless you really need them. When you do use high-frequency devices, plan your layout carefully. In very stubborn cases, you may have to lightly bypass transistor junctions with small capacitors or RC networks.

Circuits that employ local feedback sometimes necessitate careful transistor selection and use. For example, transistors operating in a local loop may require different f_Ts to achieve stability. Emitter followers are notorious sources of oscillation, and you should never drive them directly from low-impedance sources.

The circuit in **Fig 2 (Fig 5a** in **Ref 1)** employs 74C04 CMOS inverters instead of output transistors, but it too would exhibit local oscillation if it didn't include the RC damper network that's connected from the inverters' outputs to ground. The circuit forces the 74C04s to run in their linear region. Although the 74C04s' dc gain is low, their bandwidth is high. Therefore, with these ICs, very small parasitic-feedback terms result in high-frequency oscillations. The damper network provides a low-impedance path to ground at high frequencies, breaking up the unwanted feedback path.

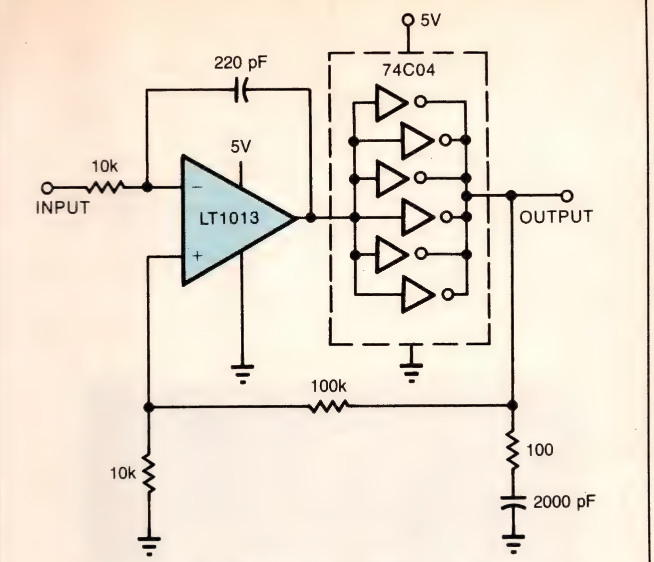
Additional delay spurs loop oscillation

Loop oscillations arise when the added gain stage supplies enough delay to force substantial input-to-output phase shift. This phase shift causes the control amplifier to run too far out of phase with the gain stage. The control amplifier's gain combined with the added delay causes oscillation. Loop oscillations are usually relatively low in frequency, typically 10 Hz to 1 MHz.

A good way to eliminate loop-caused oscillations is to limit the gain-bandwidth product of the control amplifier. If the booster stage has a higher gain-bandwidth product than the control amplifier, its phase delay is easily accommodated in the loop.

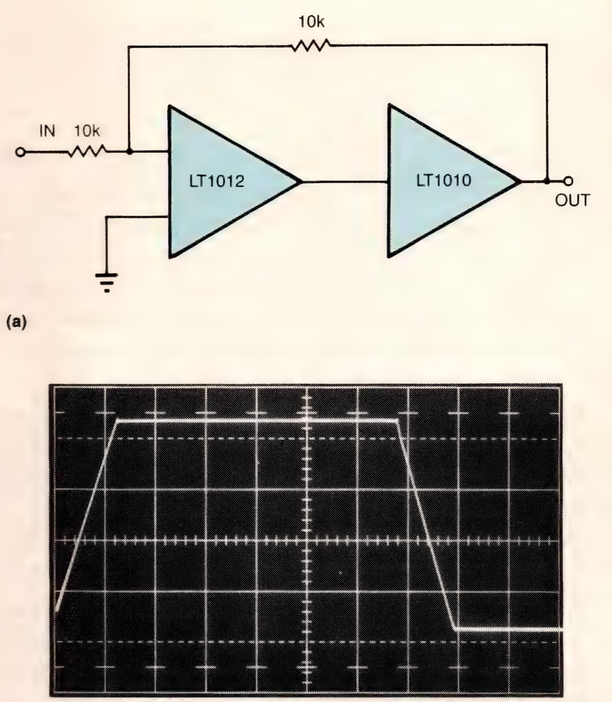
If the control amplifier's gain-bandwidth product dominates, oscillation is inevitable. Under these conditions, the control amplifier hopelessly tries to servo a feedback signal that consistently arrives too late. The servo action takes the form of an electronic tail chase, with oscillation centered around the ideal servo point.

Frequency-response roll-off of the control amplifier



LOAD (Ω)	OUTPUT SWING (V)
5k	4.92—0.00
2.5k	4.84—0.00
1k	4.65—0.00
220	3.65—0.00

*Fig 2—**The RC damper network** from the inverters' outputs to ground eliminates local oscillation.*



VERTICAL	HORIZONTAL
5V/DIV	100 μSEC/DIV

*Fig 3—**If a buffer amplifier has lower bandwidth** than the control amplifier that drives it, you probably will not encounter high-frequency oscillation. The LT1012 is only a 600-kHz unit, whereas the LT1010 buffer is a 200-MHz device.*

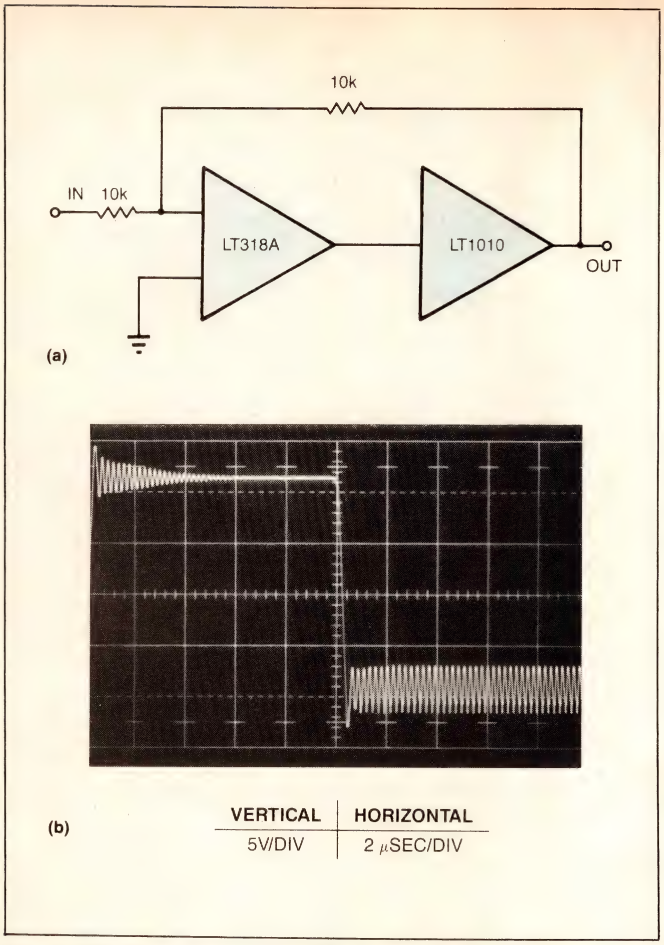


*Fig 4—**Substituting a 15-MHz LT318A for Fig 3's LT1012** results in high-frequency oscillation because the phase shift through the LTC1010 is now appreciable.*

will almost always cure loop oscillations. In many situations, brute-force compensation—using large capacitors in the major feedback loop—provides the simplest solution. As a general rule, you can stabilize the loop by rolling off the control amplifier's gain-bandwidth product. The feedback capacitor serves to trim only step response; therefore, you shouldn't rely on it to stop outright oscillation.

The 600-kHz gain-bandwidth LT1012 amplifier used with the LT1010 current buffer produces the output shown in **Fig 3.** The LT1010's 20-MHz gain-bandwidth product introduces negligible loop delay, and waveform dynamics are clean. In this case, the LT1012's internal roll-off is well below the output stage's, and you achieve stability with no external compensation components.

Fig 4 uses a 15-MHz LT318A as the control amplifier. Here, the control amplifier's roll-off, close to the output stage's roll-off, causes problems. The phase shift through the LT1010 is now appreciable, and oscillation occurs. Stabilizing this circuit requires that you degenerate the LT318A's gain-bandwidth product.

The fact that the slower op-amp circuit doesn't oscillate is a key to understanding how to compensate booster loops. With the slow device, compensation is free. The faster amplifier makes the ac characteristics of the output stage significant and requires roll-off components for stability.

The high-voltage transistors in **Fig 5a (Fig 9a, Ref 1)** are very slow devices, and the LT1055 amplifier has a much higher gain-bandwidth product than the output stage. The 10-kΩ/100-pF network is locally compensated for by the LT1055, giving it an integrator-like response. This compensation, combined with the damping provided by the 33-pF feedback capacitor, affords good loop response.

Without any compensation components installed, the circuit oscillates **(Fig 5b).** The relatively slow oscillation frequency suggests a loop-oscillation problem. The RC components around the LT1055 degrade its gain-bandwidth product.

In this case, an RC time constant eliminates oscillations and gives the best possible response **(Fig 5c)** with no loop-feedback capacitor in place. Observe that the 1-μsec time constant selected offers significant attenuation at the oscillation frequency noted in **Fig 5b.** Finally, the loop-feedback capacitor selected (33 pF) gives the optimum damping, as depicted in **Fig 9b** of **Ref 1.**

When using compensation designs such as these, remember to investigate the effects of various loads and output operating voltages. Sometimes a compensation scheme that appears fine gives bad results for some output conditions. For this reason, you should check the compensated circuit over as wide a variety of operating conditions as possible. **EDN**

Reference

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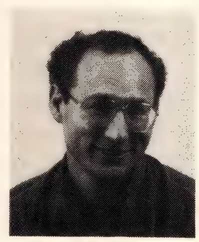
Author's biography



Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at MIT. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
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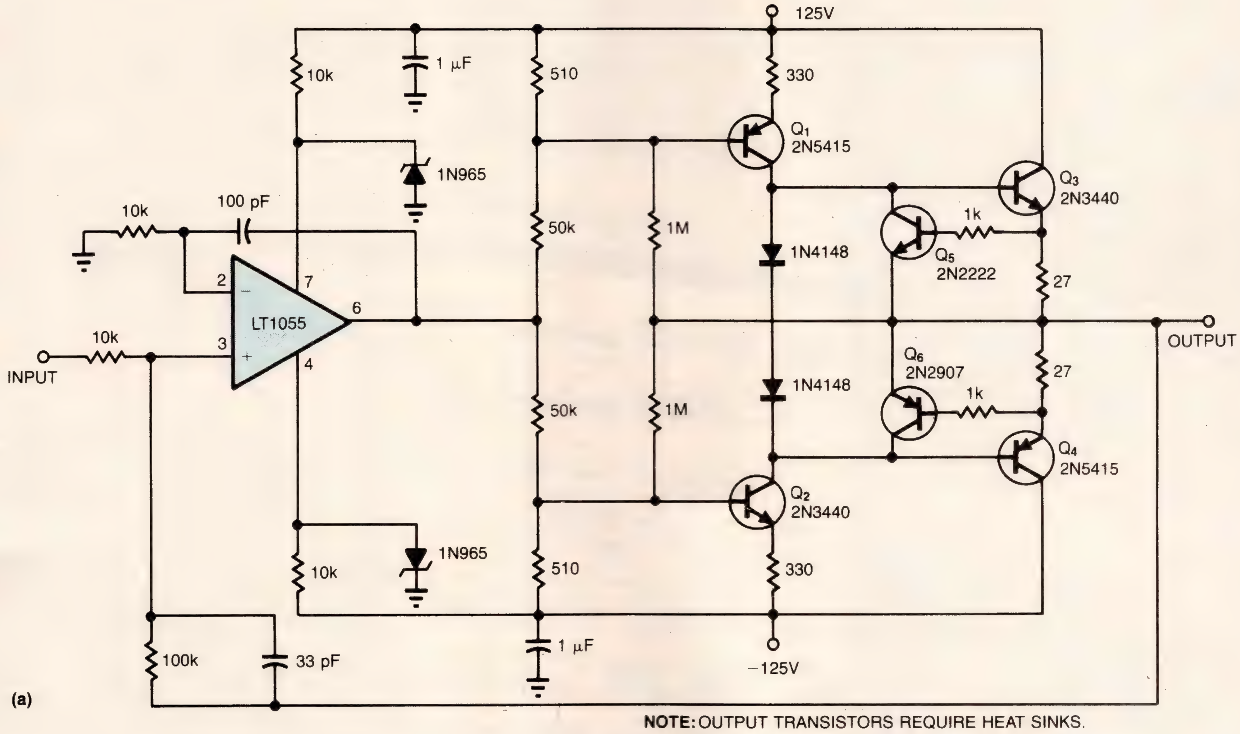
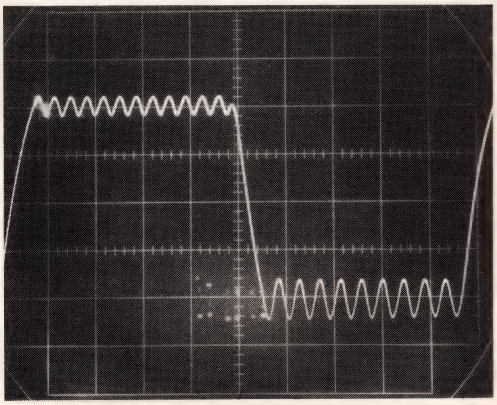
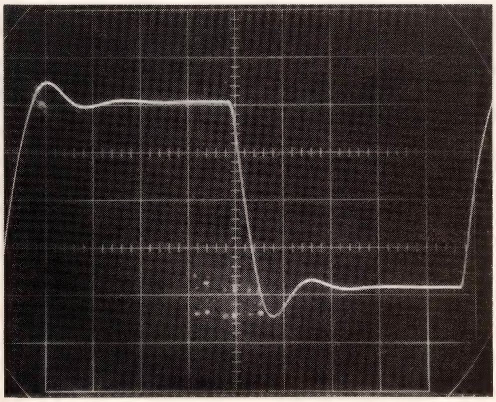
The output stage's added gain and phase shift can cause poor ac response or outright oscillation.





VERTICAL	HORIZONTAL
50V/DIV	10 µSEC/DIV

(b)



VERTICAL	HORIZONTAL
50V/DIV	10 µSEC/DIV

(c)

***Fig 5—This circuit (a) oscillates (b)** when no compensation components are installed. The relatively slow oscillation frequency suggests a loop-oscillation problem. With the attenuation components in place, the 1-µsec time constant yields both the best possible response and significant attenuation of the spurious oscillation **(c)**.*

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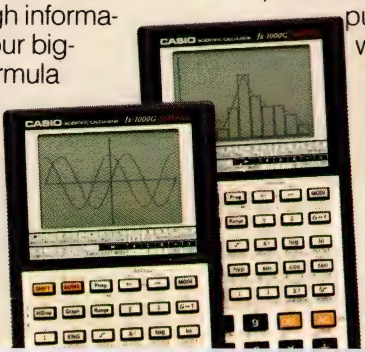

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CIRCLE NO 140

Annunciator gives audible pulse count

Charles Mitchell
Elcotel Inc, Sarasota, FL

The circuit shown in **Fig 1** not only counts pulses; by connecting the audio output to a suitable amplifier and speaker, you'll receive a voice report on the total count (nine or less) when you depress switch S_1.

TTL-level negative-going pulses feed into the counter (IC_1), which provides a corresponding binary input to the speech processor (IC_2). The processor requires a 3.12-MHz crystal (Y_1) to regulate its internal clock frequency. Also, the processor contains data for the words "oh" (0000, for zero), "one" (0001), "two" (0010), and on through "nine" (1001). When it's not busy talking (ie, when pin 8 is low), the processor responds to a low signal on pin 20 by loading its input word (A_1 through A_8) and annunciating the appropriate digit at its output (pin 24). This output is a pulse-width-modulated digital speech signal that requires a 5-kHz lowpass filter (R_2, C_2, R_3, and C_3). C_4 is a dc-blocking capacitor; R_1 and C_1 provide a power-up reset for the speech chip. **EDN**

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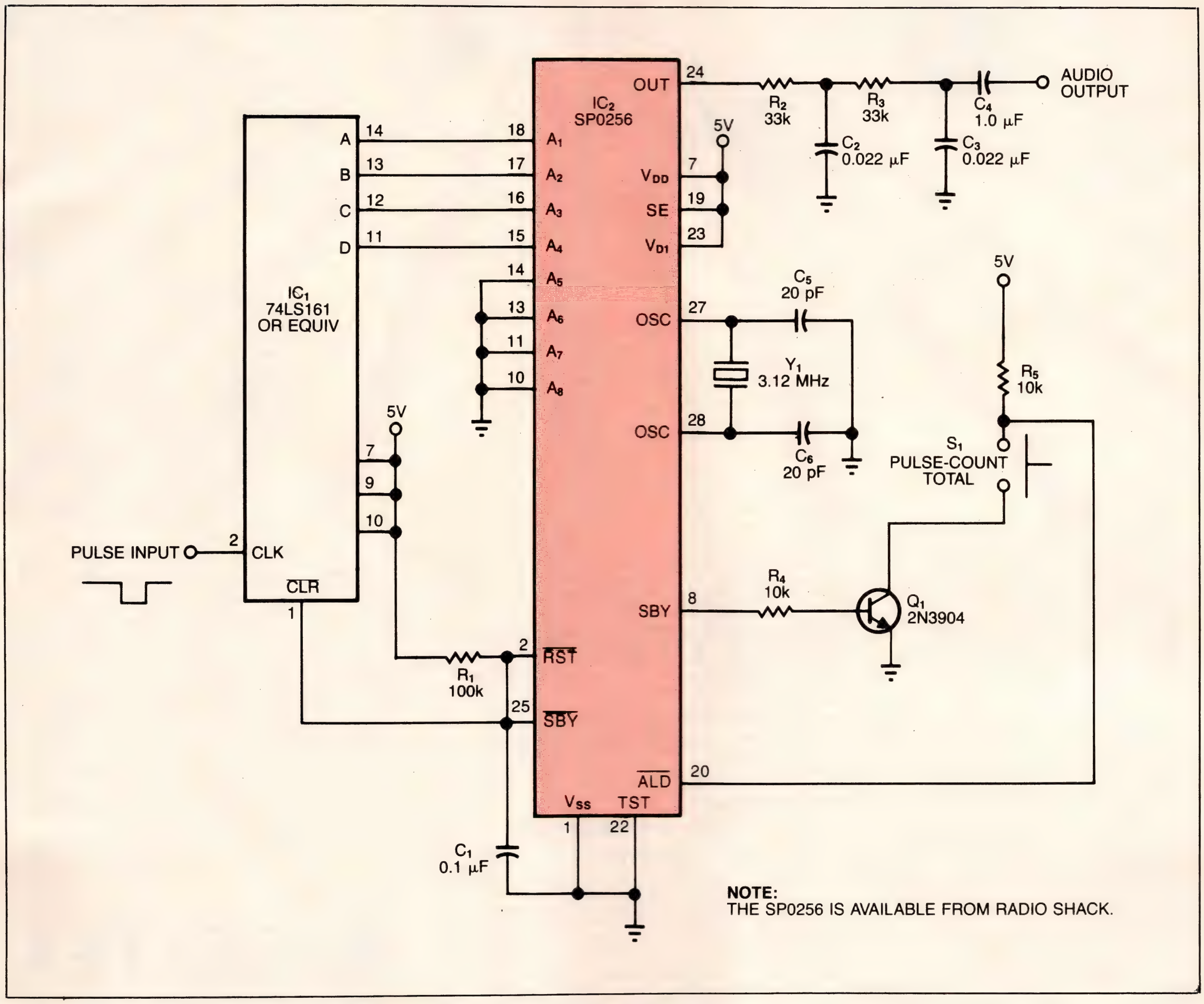
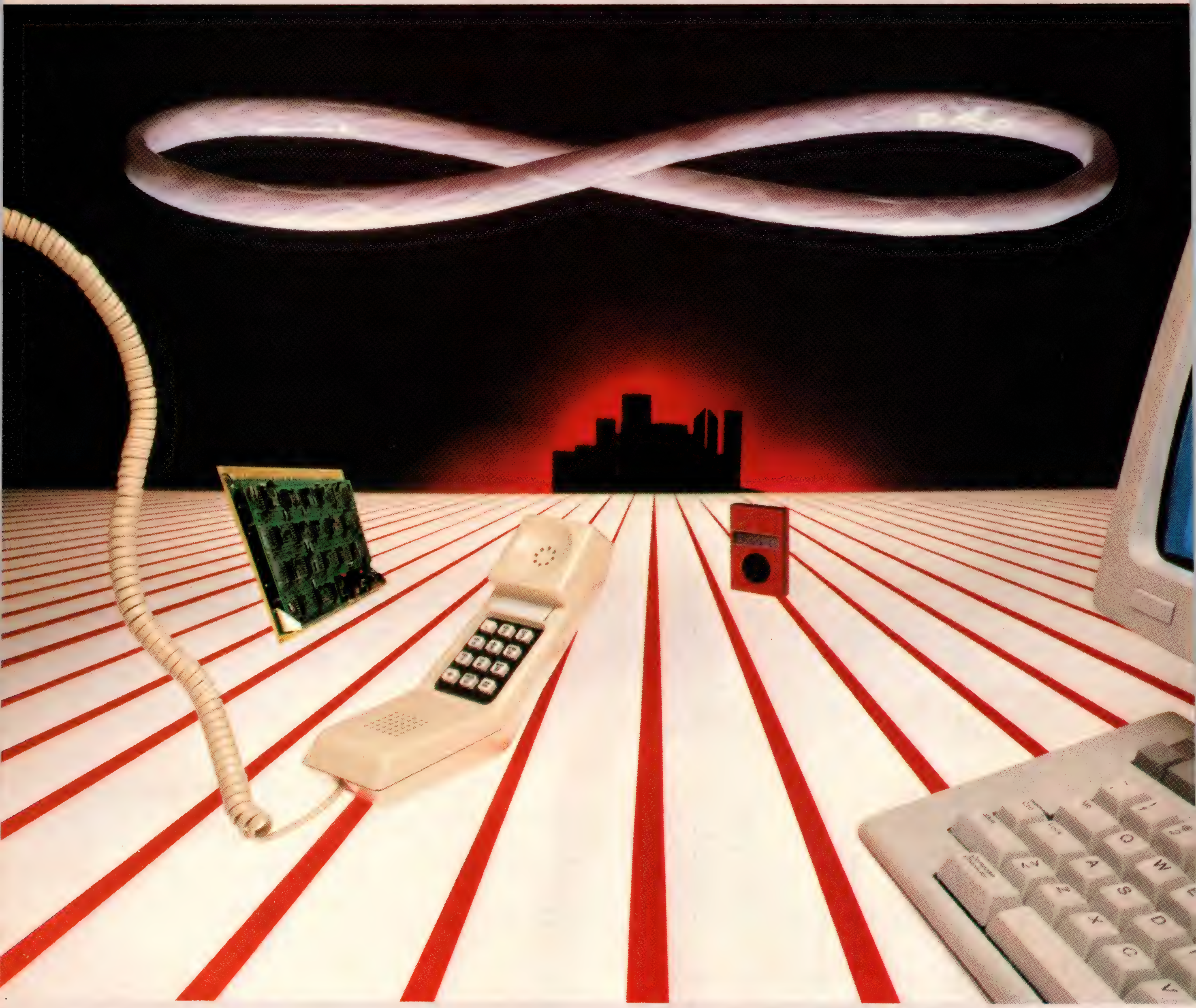


Fig 1—Speech-processor chip IC_2 provides an audible annunciation of this circuit's input pulse count.

S O L T E X



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CIRCLE NO 120

AC circuit breaker has adjustable threshold

Kurt French
C F Electronics Inc, Commack, NY

Protecting sensitive electronic equipment from ac overcurrent conditions in the 100 to 300% range often proves to be difficult. At 125% of rated current, for example, a so-called "fast-acting" breaker probably won't trip at all (**Fig 1**), and a fast-acting fuse takes about 10 sec to blow. The fuse will blow in 0.02 sec at 300% of rated current, but damage can occur at that current level. The fast-acting breaker requires nearly 700% of rated current to respond in 0.02 sec.

The adjustable circuit breaker shown in **Fig 2** responds in 0.02 sec under all conditions (provided you select a fast relay for K_1). For moderate overload conditions, then, it's preferable to the fuse or the fast-acting breaker. The toroid transformer (T_1) senses ac load current and produces an ac signal at the wiper

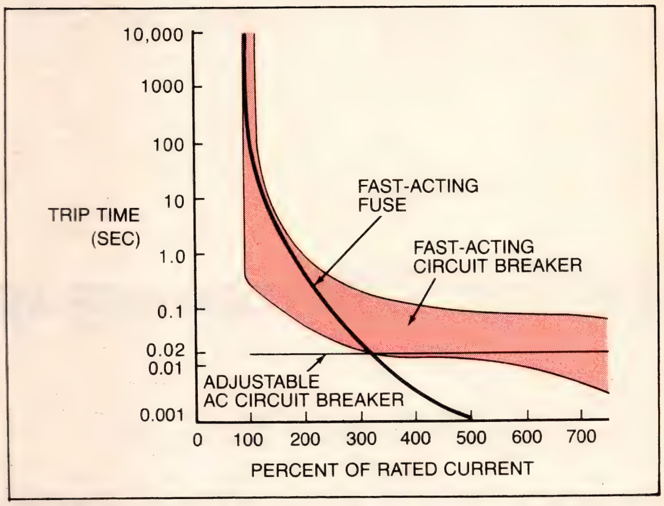

*Fig 1—**The adjustable ac circuit breaker** shown in **Fig 2** is faster than a so-called "fast-acting" circuit breaker or a fuse under moderate overload conditions.*

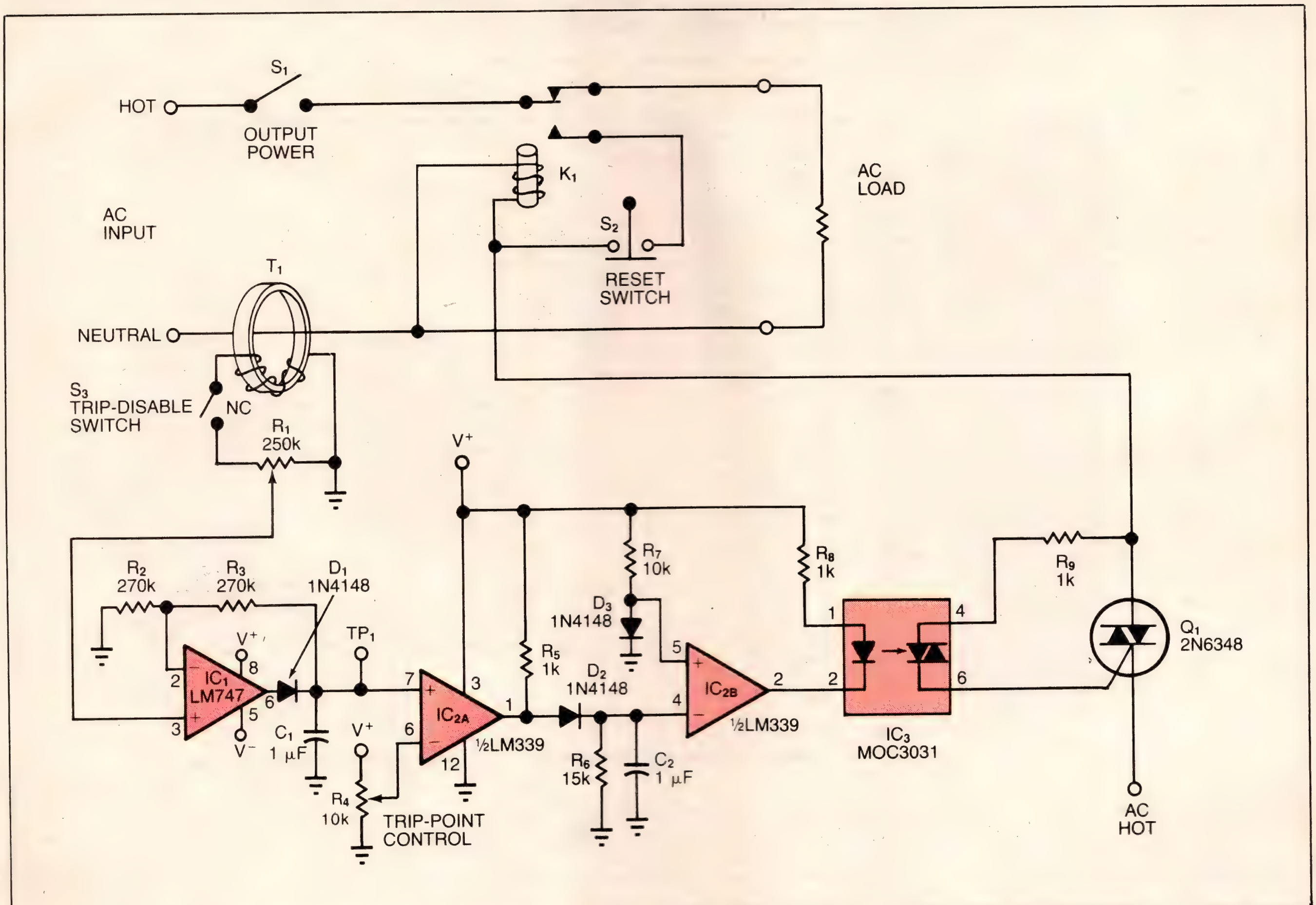

*Fig 2—**This ac circuit breaker features** an adjustable trip point, high speed, and a fast relay controlled by an optically isolated triac. If you need additional protection for heavy overload conditions, you can connect a fast-acting fuse.*

of R_1 when switch S_3 is closed. Diode D_1 rectifies this signal to produce a positive voltage at the test point (TP_1). Because R_1 allows you to calibrate this voltage, the circuit accommodates a variety of current-sense transformers.

To calibrate the trip threshold, you apply the maximum expected overload and adjust R_1 until the TP_1 voltage is 0.7V below the positive saturation level for IC_1. Then you adjust R_4 for the desired trip point. To reset the circuit breaker after it has tripped, you must open S_1 or S_2. **EDN**

To Vote For This Design, Circle No 749

Enlarge Z80 memory space to 512k bytes

Joseph G Vazach
Allen-Bradley Co, Highland Heights, OH

The circuit described here expands the Z80 µP's 64k-byte memory space to 512k bytes by switching among sixteen 32k-byte banks. The approach allows you to run programs larger than 64k bytes for applications that can tolerate an I/O operation each time the program crosses one of the 32k-byte boundaries.

The Z80's lower 15 address lines **(Fig 1)** provide access to the 32k-byte common bank of memory. The sixteenth line (A_{15}) signals any attempt to access a memory location above $7FFF_{HEX}$ (the 32k-byte limit) by activating four additional bits (A_{15} through A_{18}). Consequently, the system can access 2^{19}, or 512k, unique memory locations.

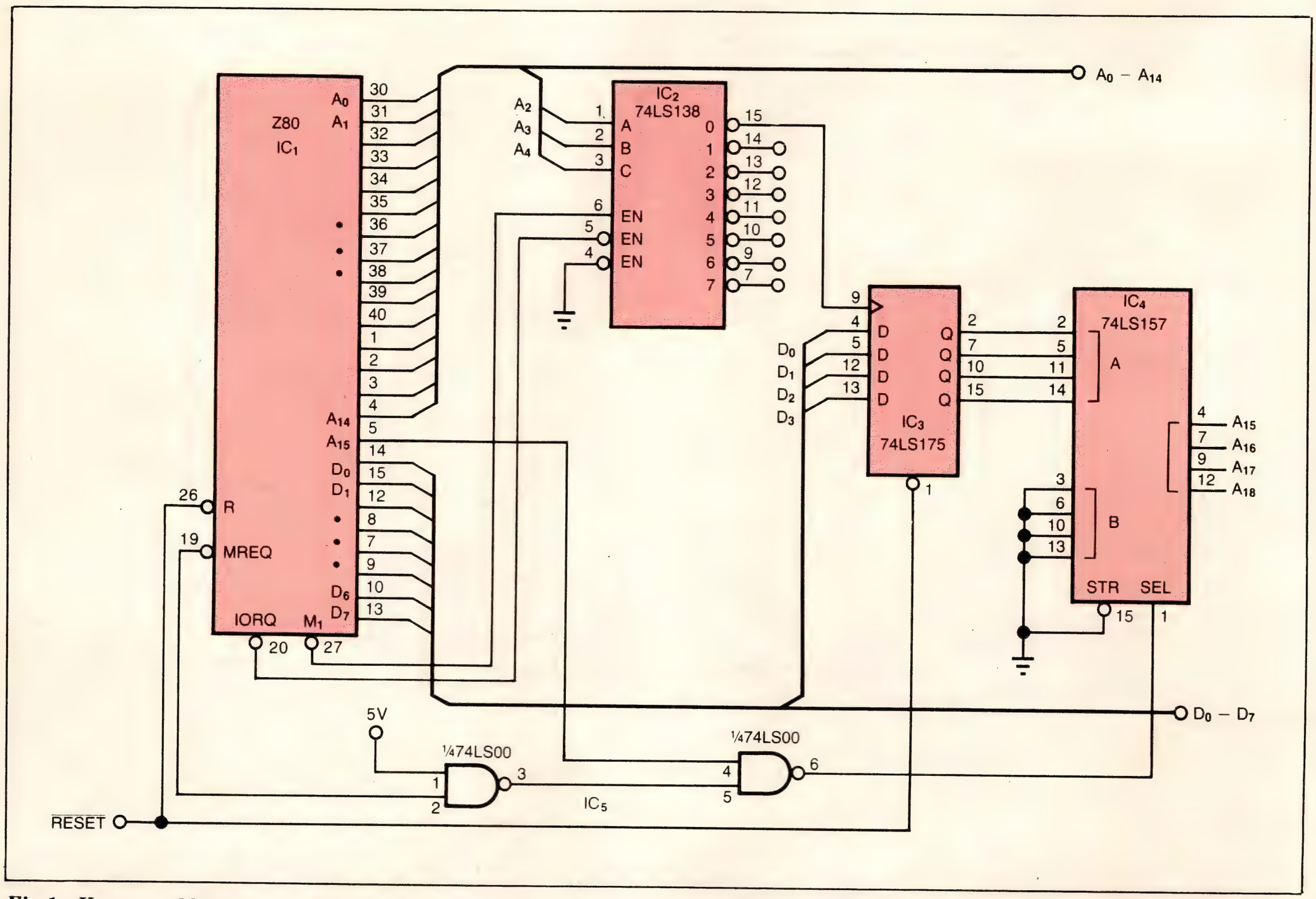

Fig 1—You can add an external bank-select register (IC₄) to increase Z80 memory space from 64k bytes to 512k bytes.

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	end, min.	200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
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*Prefix P for pins, B for BNC, N for Type N, S for SMA   example: PLP-10.7   **CIRCLE NO 121**

C105 REV. ORIG.

Your program must perform a 4-bit I/O write operation each time you access program steps or data in another memory bank. During this operation, IC_2 decodes A_2 through A_4 and strobes IC_3, which latches the data bits D_0 through D_3. Meanwhile, a logic one on A_{15} switches the quad 2-1 data selector (IC_4), causing these data bits to appear at A_{15} through A_{18}. **Fig 2** shows the physical addresses produced by combining the Z80 address with different values of IC_4, which functions as a bank register. You can return from any memory bank to the common bank (0000_{HEX} through FFF_{HEX}) without an I/O operation by simply issuing a Z80 address below 8000_{HEX}.

A reset signal latches 0000 into IC_2 and sets the Z80 to address 0000_{HEX}, yielding a starting address of 00000_{HEX}. You should also note that the Z80's M_1 line must enable IC_2 as shown to prevent a spurious signal to the IC_3 latch circuit during an interrupt-acknowledge cycle. **EDN**

To Vote For This Design, Circle No 746

Z80 ACTUAL ADDRESS < 8000	Z80 ACTUAL ADDRESS > 8000	BANK REGISTER	PHYSICAL ADDRESS
X		0	*
	X	0	*
X		1	*
	X	1	08000-0FFFF
X		2	*
	X	2	10000-17FFF
X		3	*
	X	3	18000-1FFFF
X		4	*
	X	4	20000-27FFF
X		5	*
	X	5	28000-2FFFF
X		6	*
	X	6	30000-37FFF
X		7	*
	X	7	38000-3FFFF
X		8	*
	X	8	40000-47FFF
X		9	*
	X	9	48000-4FFFF
X		A	*
	X	A	50000-57FFF
X		B	*
	X	B	58000-5FFFF
X		C	*
	X	C	60000-67FFF
X		D	*
	X	D	68000-6FFFF
X		E	*
	X	E	70000-77FFF
X		F	*
	X	F	78000-7FFFF

*REPRESENTS THE COMMON BANK OF PHYSICAL ADDRESSES (00000_{HEX} THROUGH $07FFF_{HEX}$).

Fig 2—Loading the appropriate 4-bit word *in the bank register of* ***Fig 1*** *lets you select one of 16 different 32k-byte memory banks.*

Op amp provides dc bias for transistor

Norman M Hill
Zetron Inc, Bellevue, WA

Microwave transistors require a proper dc bias, as do most transistors that perform ac amplification. An op amp can set this bias by actively regulating the collector's dc current and voltage. **Fig 1** illustrates an example of the technique.

Feedback from op amp IC_1 in **Fig 1**'s circuit adjusts the transistor's dc base current to maintain a V_C of 10V, which in turn sets the dc collector current at 20 mA. The op amp is configured as a difference integrator that renders V_C equal to V_R. Because the integrator's phase lag is a constant 90°, the feedback loop is quite stable. Furthermore, the loop's time constant is about 0.1 sec; you can speed this response by reducing the integrator's resistor or capacitor values (R_3, R_4, C_1, and C_2).

The collector current depends directly on the value of R_1, but the tolerance of other component values is not critical. The typical base current should produce about 4V across R_5. **EDN**

To Vote For This Design, Circle No 748

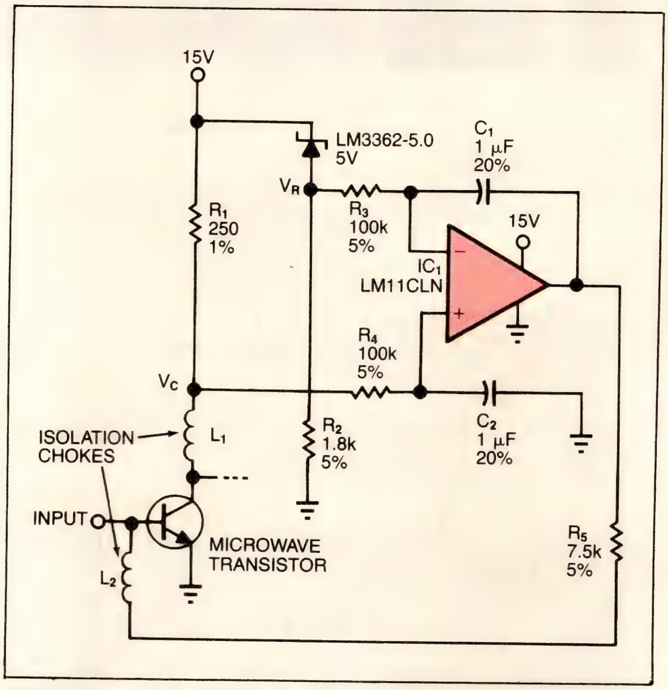

Fig 1—Op-amp feedback actively regulates *a microwave transistor's dc bias point by adjusting the transistor's dc base current, which in turn maintains a stable dc collector current.*

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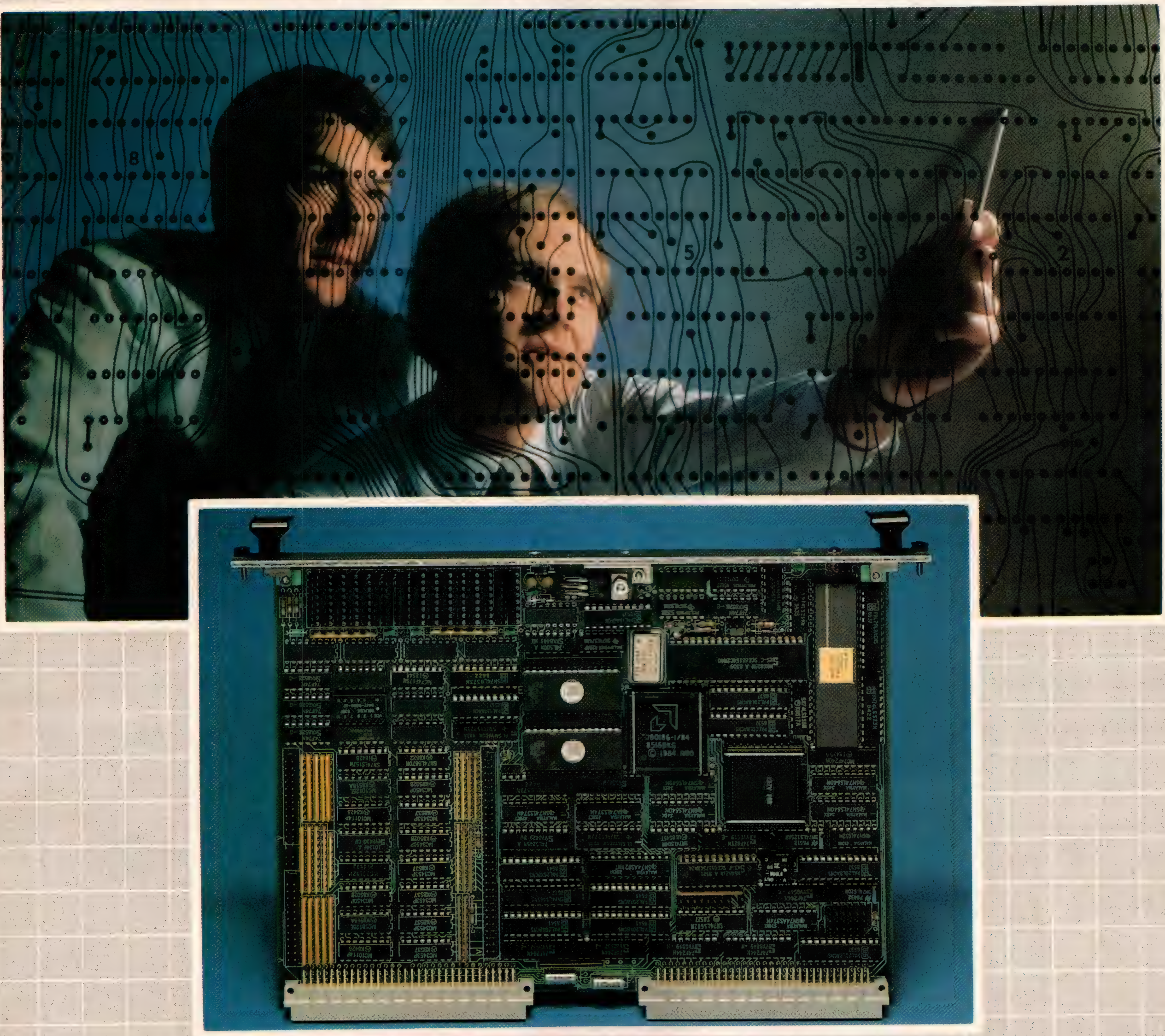

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CIRCLE NO 124

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Precision circuit increases ADC resolution

James M Bryant
Analog Devices, Newbury, Berkshire, UK

By detecting an analog signal's polarity and inverting the signal when necessary, you can transform the output code of a conventional, unipolar A/D converter from straight binary to sign-magnitude code, and you'll add one bit of resolution in the process. You achieve this goal by preceding the converter with a modulus circuit that provides a digital polarity indication **(Fig 1)**.

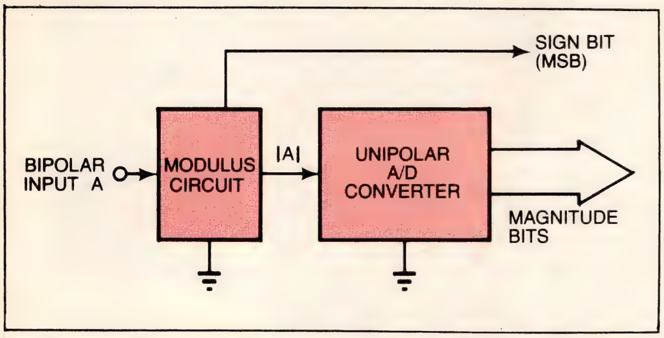

Fig 1—A modulus circuit converts a bipolar analog signal *to a unipolar signal and generates a sign bit, allowing a unipolar A/D converter to produce sign-magnitude output code.*

The modulus circuit (IC_1 in **Fig 2**) is a balanced-modulator/demodulator chip configured as a unity-gain absolute-value amplifier. The input (A) goes to a comparator that senses polarity with respect to ground and switches the circuit gain to +1 or −1 as appropriate. R_1, R_2, and R_3 allow you to null the comparator's offset voltage. (If the offset is acceptable to you, however, remove these resistors and connect pin 10 to ground.) **EDN**

To Vote For This Design, Circle No 750

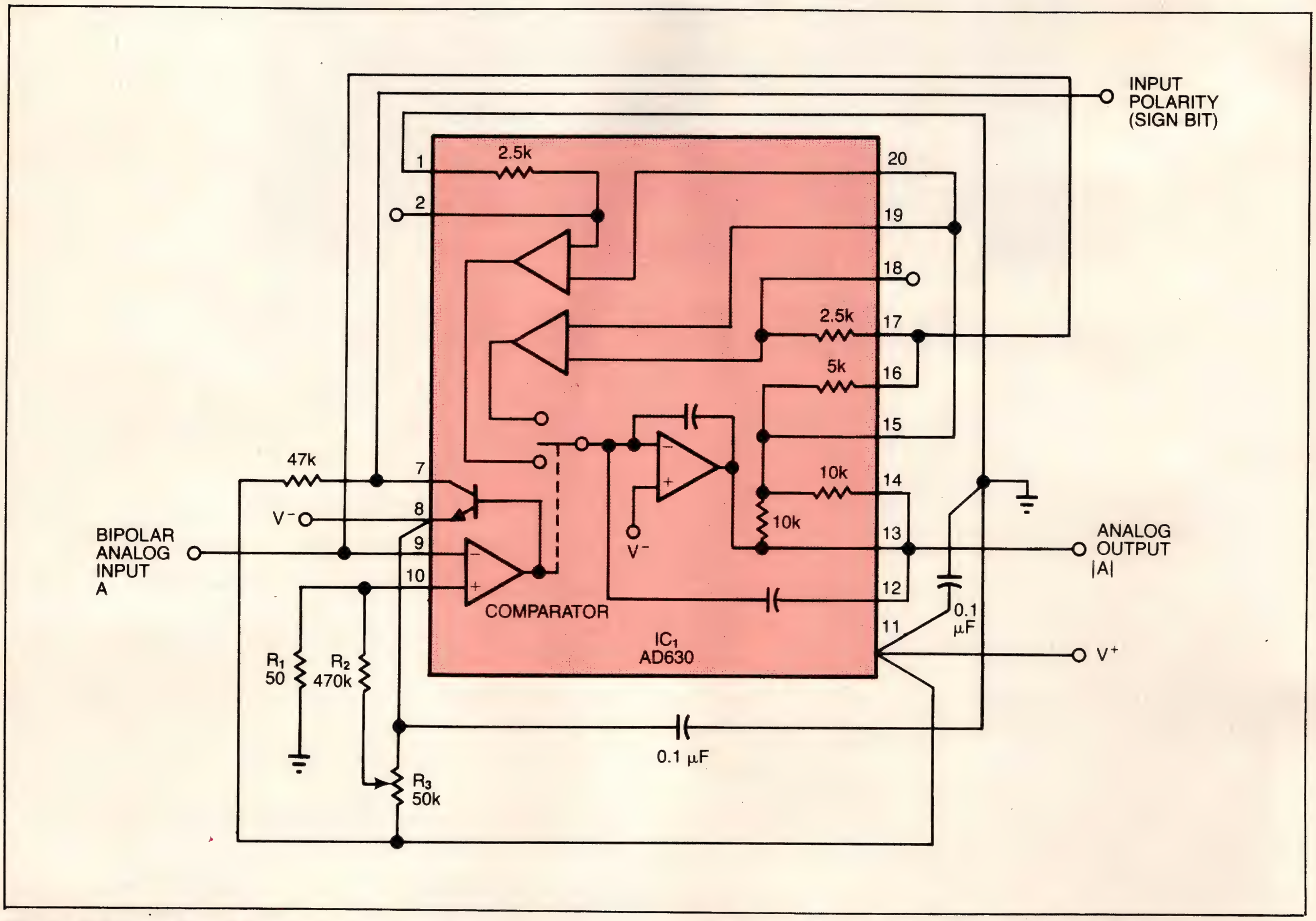

Fig 2—A balanced modulator chip *configured as an absolute-value amplifier serves as the modulus circuit shown in* ***Fig 1.***

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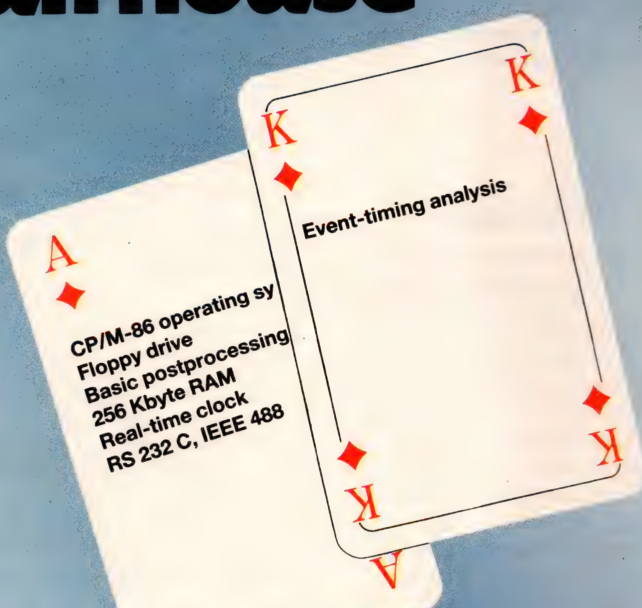

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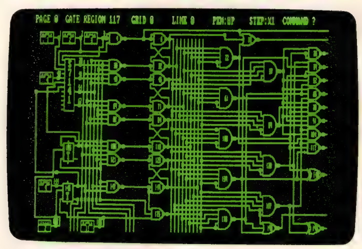

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CIRCLE NO 122

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The Bitgrade fault simulator grades test patterns for self-testing digital circuits much faster than general-purpose fault simulators, according to the manufacturer. The program's modeling scheme divides circuits into combinatorial logic and response-accumulation logic. Proprietary simulation algorithms accelerate the simulation of faults in the combinatorial logic. A circuit-description language speeds the specification of your self-test scheme. The software models transistors and gates. Versions are available for Apollo, Sun, and VAX workstations and IBM mainframes. One-time license fee, $25,000 to $100,000.

Gateway Design Automation Corp, Box 1545, Littleton, MA 01460. Phone (617) 486-9701.

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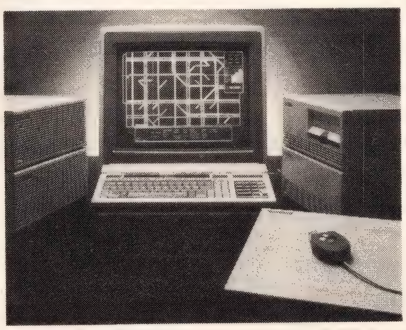

PC-BOARD LAYOUT

The HP Printed Circuit Design System couples pc-board layout with design, manufacturing, and testing. The system runs on HP 9000 Series 300 technical workstations under the HP-UX operating system. The company has licensed the package's source code from Bell Northern Research. (This package is based on Bell Northern's Circuit Board Design System.) To enter a net list, you can transfer data from the company's logic design system or its engineering graphics system, as well as from any system that uses the Electronic Design Interchange Format, to the layout system. The system automatically positions logically connected gates as close together as possible. The component library provides nearly 4500 digital and analog parts. Parts with common outlines share space in the database. During a route, you can check the progress of automatic routing; the router can use 50-, 25-, and 20-mil grids. A look-ahead algorithm plans routing strategies. When your design is complete, the system generates photoplotter instructions, N/C drill tapes, and production reports. $60,000 to $82,000 including hardware. Delivery, 12 to 16 weeks ARO.

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Circle No 351

LOGIC SIMULATOR

In addition to schematic capture, the Validation Designer AT simulates logic and verifies timing for digital circuits. The package also generates net lists. The system includes an IBM PC/AT, which features an 85M-byte hard-disk drive, an optical mouse, a 32-bit coprocessor with 2M bytes of RAM, and Unix System V. The coprocessor runs this company's Unix-based CAE software. You can toggle between Unix and PC-DOS, mixing CAE tasks with standard IBM operations. The CAE software can use the company's gate-array, standard-cell, and pc-board libraries to model ASIC and system designs. You can simulate designs as large as 5000 gates on the system. For larger designs, you can create the schematic on the PC/AT and transfer the design to another system via Ethernet. Three graphics display options are available. The Model AT/GX includes the IBM color display with 1024×1024-pixel resolution. The AT/EG version uses the IBM enhanced color display and adapter (a 13-in. display with 640×350-pixel resolution). The AT/VG model features the manufacturer's display and subsystem, which provides a 15-in., 1024×800-pixel display. AT/GX, $36,950; AT/EG, $27,950; AT/VG, $29,950.

Valid Logic Systems Inc, 2820 Orchard Parkway, San Jose, CA 95134. Phone (408) 945-9400. TLX 3719004.

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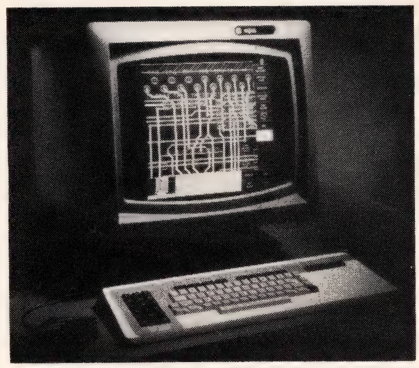

CAE/CAT TOOLS

The Logic Series of CAE and CAT tools comprises three packages: Logic Scribe, a schematic-entry and project - management program; Logic Explorer, an interactive design-analysis and -verification program; and Logic Examiner, an interactive test-development and -verification program. Logic Scribe includes an interactive monochrome- or color-graphics editor. It also provides communications facilities for data transfer between Apollo and VAX, Data General, or other Apollo systems. In addition to the capabilities of the first package, Logic Explorer provides a mixed-level logic simulator. It also calculates a relative measure of design testability based solely on circuit topology. Logic Examiner combines elements of the other packages with a fault simulator. Also included is an interface to the IMS Logic Master for prototype testing, as well as interfaces to such production testers as GenRad's GR-16, GR-18, and L-135 or Fairchild's Sentry V, Sentry VII, and Sentry XX. The packages are available either as unbundled software or bundled on Apollo workstations. Logic Scribe, $19,400 (Apollo 3000 monochrome) or $27,300 (3000 color); Logic Ex-

plorer or Logic Examiner, $50,000 (3000 monochrome), $58,000 (3000 color), or $82,000 (Apollo DN570A).

GE Calma, 501 Sycamore Dr, Milpitas, CA 95035. Phone (408) 434-4000. TWX 3720067.

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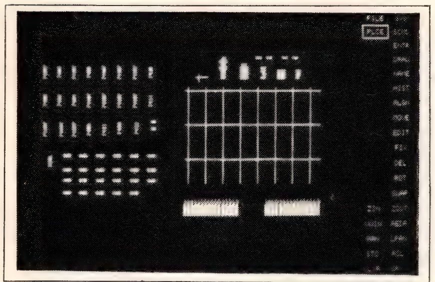

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Personal CAD Systems Inc, 1290 Parkmore Ave, San Jose, CA 95126. Phone (408) 971-1300.

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Factron EDA, 269 Mt Hermon Rd, Suite 105, Scotts Valley, CA 95066. Phone (408) 438-2880. TLX 855538.

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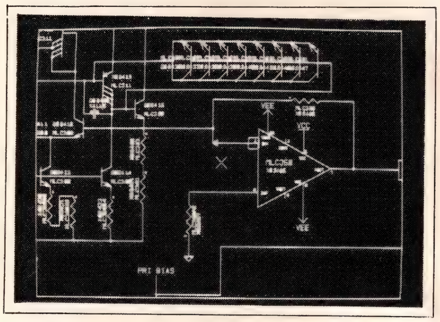

LINEAR-IC DESIGN

Linear CAD II, a linear-design program, runs on IBM PC/XTs or PC/ATs that contain 512k bytes of RAM and an 8087 math coprocessor. In addition to the 17 previously available macro cells, the package now includes 12 FB300-based macro cells. Among these cells are a video amplifier that's functionally equivalent to the NE592 and a timer macro cell equivalent to the NE555. The program also now provides models of the company's 12V linear bipolar process. The software includes Case Technology's schematic-capture software and MicroSim's PSpice circuit simulator. The circuit simulator can automatically handle substrate and epitaxial-tub bias. A postprocessor displays PSpice output on your computer's screen. A file-management structure optimizes the use of disk space; you can access DOS directly from the graphics editor. $10,000.

Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 262-5200.

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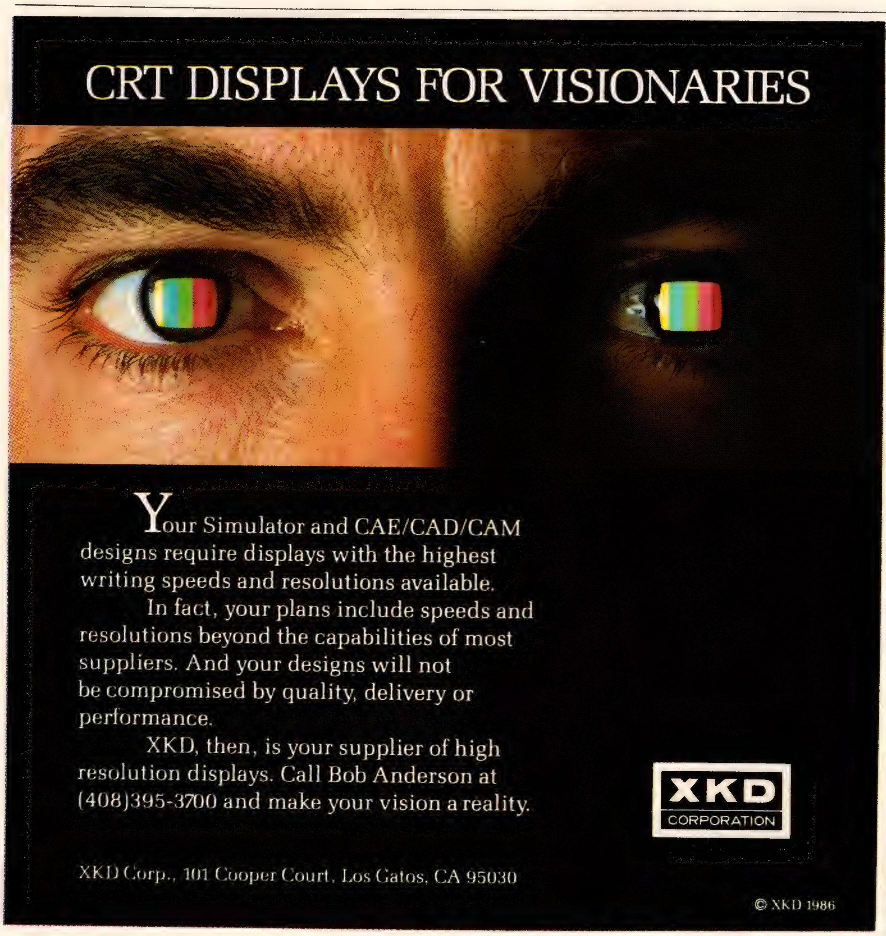
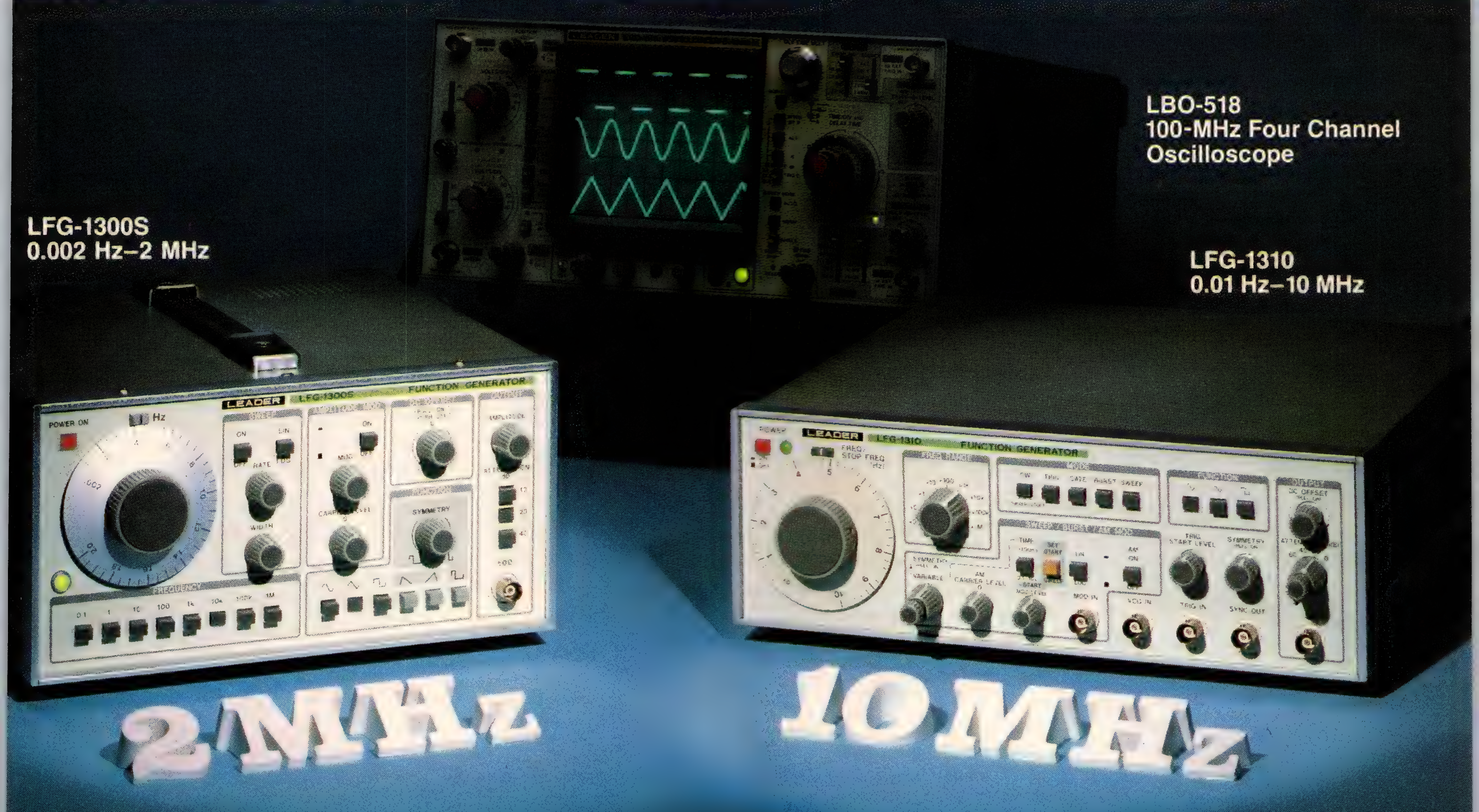


CIRCLE NO 127

LEADER



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The SuperSet 5000 VLSI design system, which runs on Apollo Domain workstations, integrates design databases from initial floor plan to final layout. The package's modules consist of BaseSet, a mandatory infrastructure program; StrucSet for schematic capture; SimuSet for mixed-mode, multilevel, and analog simulations; TopSet for symbolic hierarchical topologies; and GeoSet for geometric design. The GluSet and PlaSet modules automatically generate glue-logic and logic-array layouts. The required BaseSet contains a design database manager. You can buy either the software or a turnkey system that includes an Apollo workstation. For a typical turnkey configuration, the price per user is approximately $80,000.

Clarity Systems Inc, 710 Lakeway, Suite 290, Sunnyvale, CA 94086. Phone (408) 730-1381.

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ValidFlat translates hierarchical designs into flat designs. The software allows you to take advantage of the speed and accuracy inherent in hierarchical design techniques and still document your designs with explicit definitions of each component, wire, and interconnection. You can create original schematics with full hierachy, replication of components, and any other tools available in the design methodology. The software then produces all necessary bottom-level schematics, including pin-to-pin mapping of the physical design and back annotation. What's more, the package generates a cross-reference list of components and signals in the flat drawings. $10,000.

Valid Logic Systems Inc, 2820 Orchard Parkway, San Jose, CA 95134. Phone (408) 945-9400. TLX 3719004.

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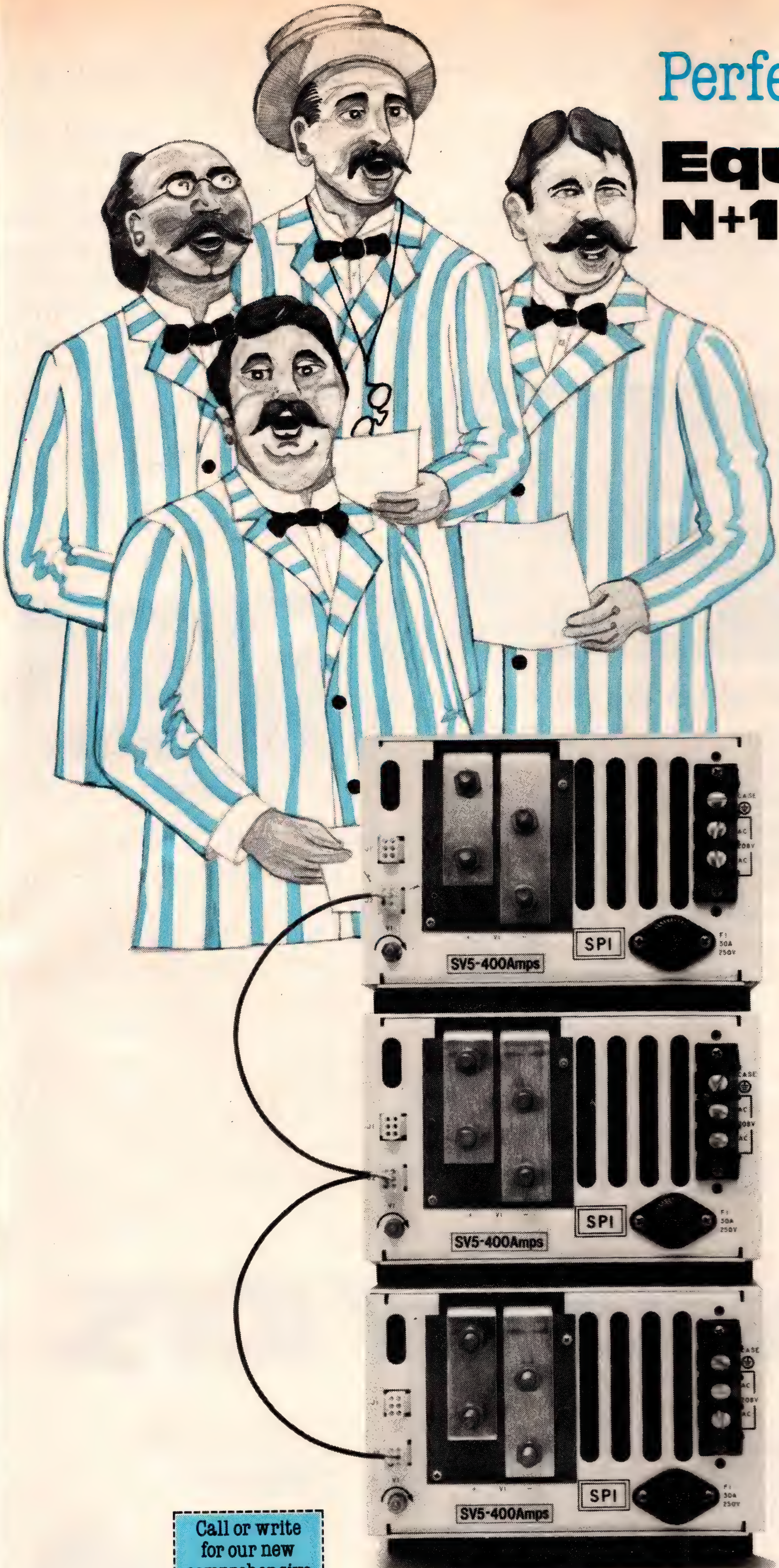

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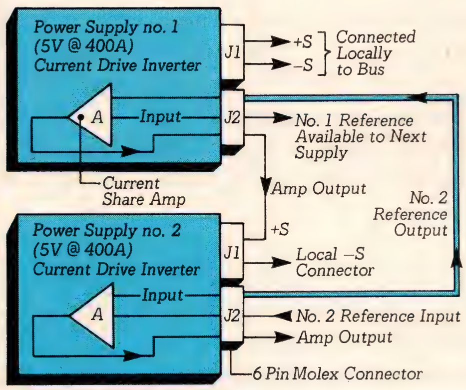

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GridComm Inc, 20 Old Ridgebury Rd, Danbury, CT 06810. Phone (203) 790-9077.

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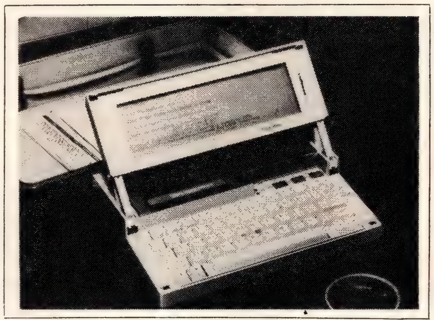
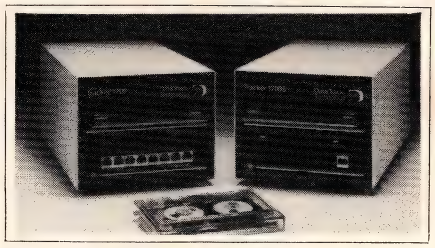


PORTABLE TERMINALS

Members of the Silent-700 family of computer products — the Travelmate, Travelmate-1200, and Travelmate-DT portable display terminals—contain User Interface Module (UIM) cartridges that let you tailor any one of the terminals to your particular needs. By formatting frequently used reports and forms, for example, into a UIM cartridge, you can develop menu-driven displays that ease data-entry and -transmission tasks. The Travelmate comes with an internal 300-baud modem. The 1200 model incorporates an internal 300/1200-baud modem. The desktop DT model contains an RS-232C interface. Each terminal has a retractable 16-line×80-column LCD, a built-in 45-cps thermal printer, a full-size keyboard, data-communications interfaces, and text editor. Travelmate, $1095; Travelmate 1200, $1295; Travelmate DT, $995.

Texas Instruments Inc, Data Systems Group, Box 809063, H-849, Dallas, TX 75380. Phone (800) 527-3500.

Circle No 360



RS-232C TAPE DRIVE

The Tracker 1700 can download unformatted and uncoded ASCII or binary data from a computer's RS-232C port and store it on a 20M-byte 3M tape cartrige. The tape drive is a true start-stop device that doesn't require you to time data transmissions through its RS-232C port or to tell it how much data you're sending. The drive handles all formatting, tape controlling, data buffer-

Continued on pg 228

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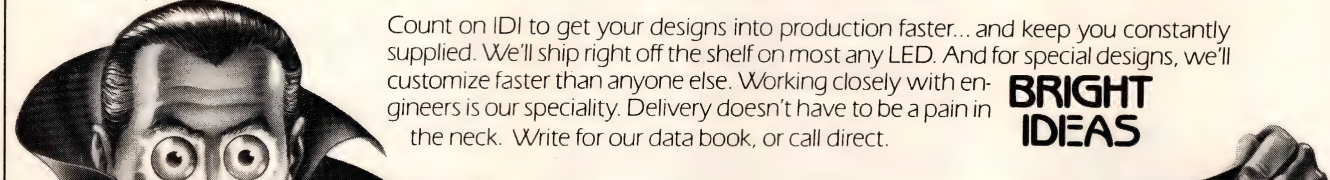

IDI Industrial Devices, Inc., Edgewater, NJ 07020
Telephone: (201) 224-4700

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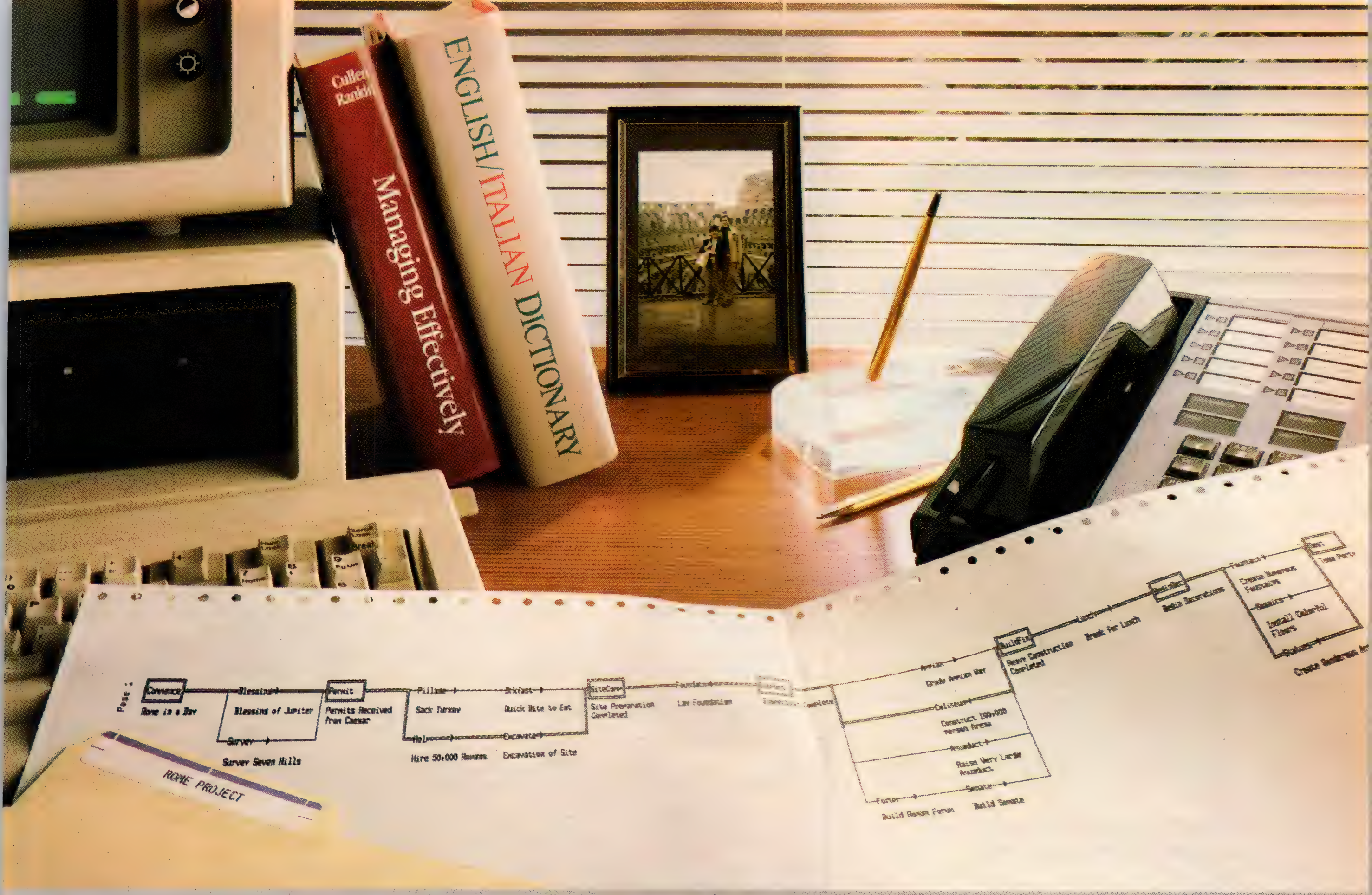

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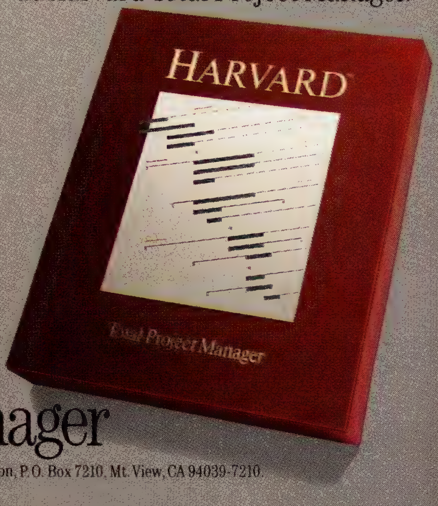

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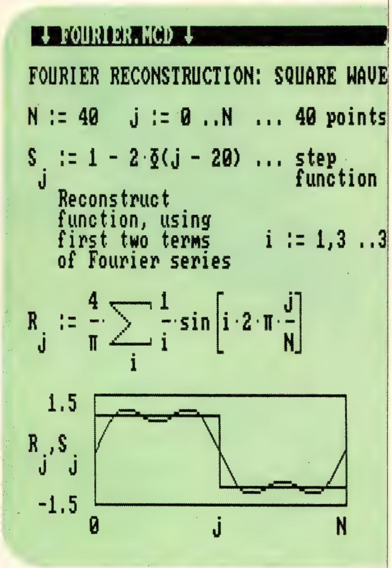

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- Many voltages available - from 19.1 to 40 volts
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Model Number	Rated				Starting Torque g-cm	No Load		Motor Constant g-cm/A	Terminal Resistance ohms
	Voltage V	Torque g-cm	Speed rpm	Current mA		Speed rpm	Current mA		
HN52-H11N1E	24	1000	2300	1350	6000	2800	120	810	3.7
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V	PRODUCT	PART NO.	ORGANIZATION	ACCESS TIME (ns)	Vcc	SUPPLY CURRENT (Max.)		PIN NO.
						ACTIVE	STAND BY	
	16K SRAM	HY61C16/L	2K x 8 BIT	45,55,70	+5V	100mA	100uA	24
		HY6116/L	2K x 8 BIT	100,120,150	+5V	100mA	100uA	24
		HY61C16A/AL	2K x 8 BIT	35,45,55	+5V	100mA	100uA	24
		HY61C67/L	16K x 1 BIT	35,45,55	+5V	50mA	100uA	20
		HY61C68/L	4K x 4 BIT	35,45,55	+5V	60mA	100uA	20
		HY61C69/L	4K x 4 BIT	35,45,55	+5V	60mA	100uA	22
	64K SRAM	HY6264	8K x 8 BIT	45,55,70	+5V	100mA	10mA	28
	64K DRAM	HY51C64/L	64K x 1 BIT	100,120,150	+5V	37mA	1.5mA	16
	256K DRAM	HY51C256L	256K x 1 BIT	100,120,150,200	+5V	55mA	2mA	16
	64K EPROM	HY27C64	8K x 8 BIT	150,200,300	+5V	30mA	100uA	28
	1K EEPROM	HY93C46	64 x 16 BIT	250KHz	+5V	4mA	400uA	8
	PEEL	HY18CV8	–	25/15	+5V	25mA	15mA	20

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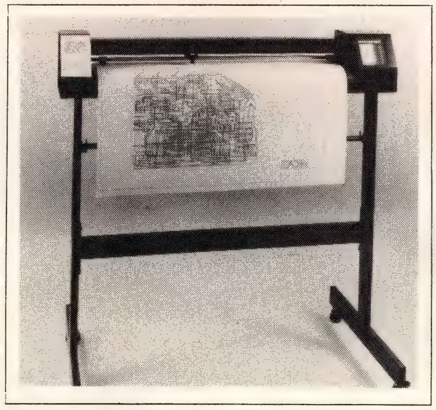

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Able to produce engineering drawings as small as the size of a business card and as large as 37.5×81 in., Model SP1200 plots on sheet or roll stock for output on paper, vellum, or transparent film. Its pen can reach speeds of 10 ips with 0.0025-in. resolution. The plotter comes with a 14k-byte buffer. The unit measures 50×10×9 in. and weighs less than 50 lbs; an optional stand increases the total height to 49 in. Using its RS-232C interface, you can connect the plotter directly to a workstation, or use it as a shared resource on a local network. In a multiuser environment, you can place the peripheral between a pc or terminal and a printer to accomplish an eavesdropping operational mode. In this mode, the SP1200 only plots when you specifically order it to do so, and it allows you to use the printer in an ordinary manner at other times. SP1200, $4995; stand, $250.

Enter Computer Inc, 6867 Nancy Ridge Dr, San Diego, CA 92121. Phone (619) 450-0601. TLX 181740.

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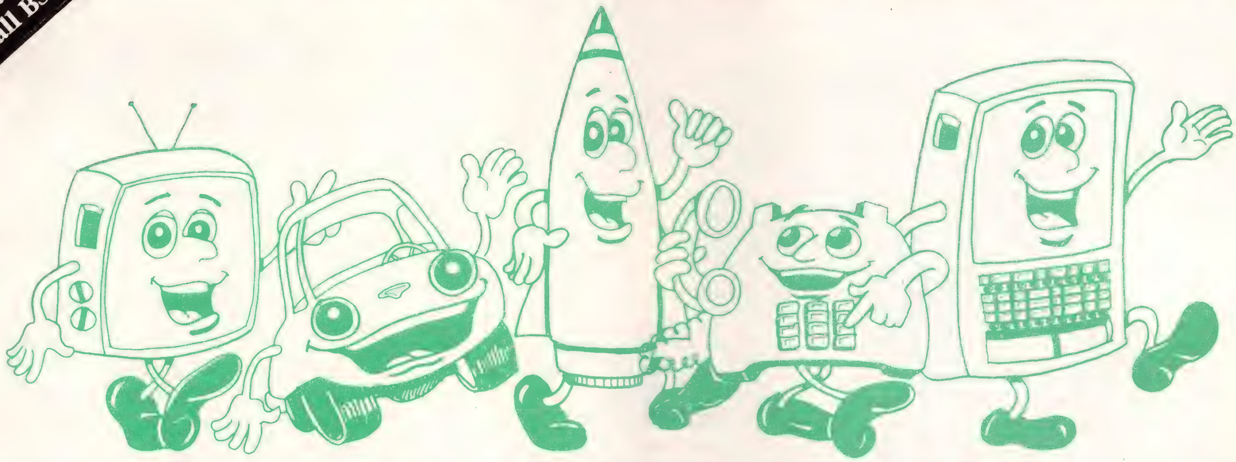

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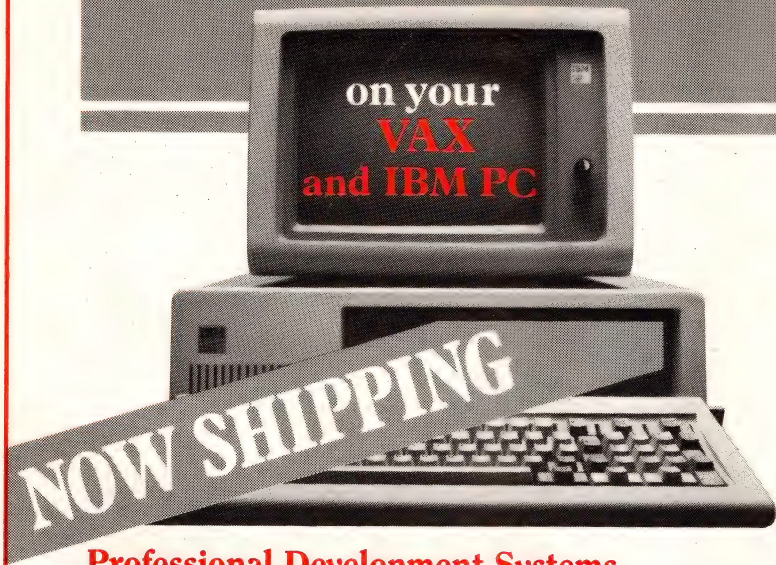

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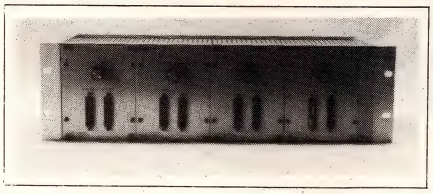

V.35 INTERFACE PATCH

The Model 9179 is a V.35 interface patch that lets you monitor high-speed data signals and reconfigure connections between modems and terminals. This module provides an access point for testing and switching when your computer equipment malfunctions or when you need to reroute data paths. You connect a 9179 module between each V.35 modem and its associated data terminal. When the module is in its normal switch setting, the modem and terminal are connected to each other and you can access their interface signals with a data-link analyzer via the module's front panel connector. When you switch the module to its patch setting, all modem and terminal signals are routed to the module's front-panel connections so you can patch in back-up equipment while making repairs to the modem-to-terminal communciations link. As many as four 9179 modules can fit into a standard 19-in. rack. $229.

Electro Standards Laboratory Inc, Box 1944, Providence, RI 02940. Phone (401) 943-1164.

Circle No 363

VIDEO MUX

The EtherVideo video multiplexer can simultaneously transmit local video and data signals over Ethernet baseband networks. Accepting both baseband and composite audio-video signals, the unit can modulate these signals to any RF carrier in the UHF frequency spectrum (470 to 770 MHz). The modulated signal passes through the multiplexer's isolating combiner to merge with the data transmissions on your Ethernet LAN. You can use this multiplexer to transmit video tapes,

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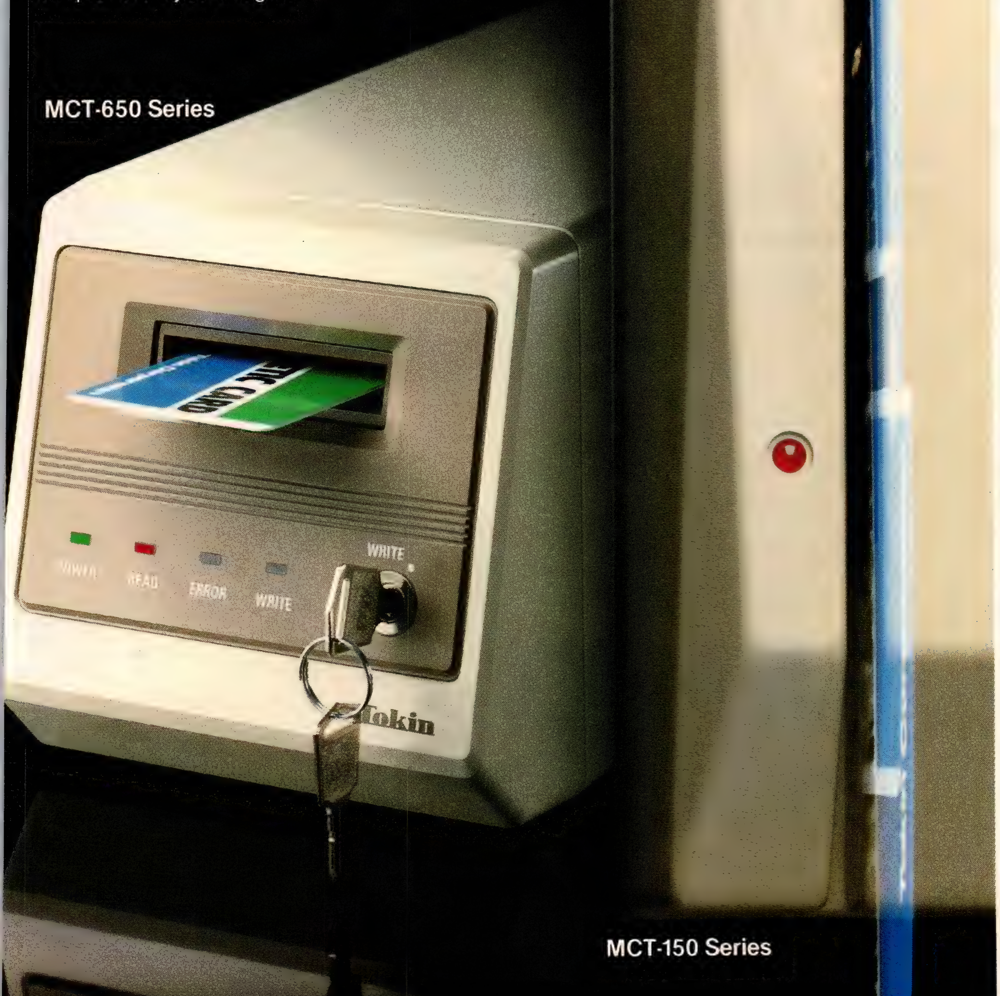


MCT-650 Series

MCT-150 Series

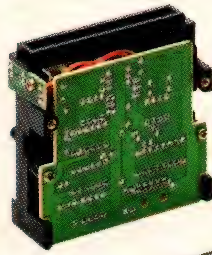
Interface of MCT-650 and MCT-150 Series

	MCT-650 Series	MCT-150 Series
Communication standards	Standard EIA, RS232C	
Communication mode	Start-stop synchronization, full duplex (half duplex)	Start-stop synchronization, full duplex
Transmission speed (baud)	1,200/2,400/ 4,800/9,600	1,200
Communication format	Start bit 1 Data bit 8 Parity (even) 1 Stop bit 1	
Card driving system	Motorized	Manual
Performance	Read/write	Read only

Applicable Magnetic Card

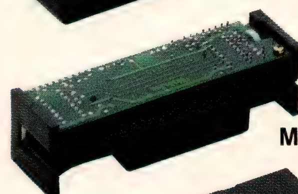
Type	Card Standard
MCS-111, 121, 131 MCI-111	ISO, track 2
MCS-112, 122, 132 MCI-112	ISO, track 1
MCS-113, 123, 133 MCI-113	ISO, track 3

Card Reader Units



MCI-110 Series

MCS-110 Series



MCS-120 Series

MCS-130 Series

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CIRCLE NO 139

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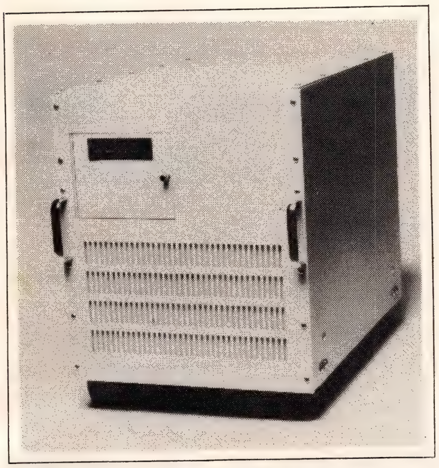
TURN TO PAGE 292

live discussions, and computer-aided instruction; to receive satellite video transmissions; or to monitor a secured area from multiple stations. It supports video signals from video tape recorders and disk players, cameras, satellite receivers, and computers. From $170.

Communication Machinery Corp, 1421 State St, Santa Barbara, CA 93101. Phone (805) 963-9471.

Circle No 364



REFRIGERATED CHASSIS

You can use the SA-H152 to protect a computer and its peripherals from the effects of a harsh environment. The SA-H152 is a closed refrigeration system in an industrial enclosure that houses a ruggedized computer chassis. The chassis includes an 8-row, quad Q-bus backplane to accommodate DEC processors and modules. Options include a backplane with 13 or 16 Q22 slots and three CD slots for MicroVAX compatibility. The enclosure has a thermostatically controlled, freon-based air-conditioning unit and air-filtration system. Its pedestal-mounted steel frame includes rubber shock mounts and casters. The unit comes with a 300W power supply, mounting for three 5¼-in. disk drives, and a front operating panel with control and status indicators. $4500.

Sigma Information Systems, 3401 E La Palma Ave, Anaheim, CA 92806. Phone (714) 630-6553. TLX 298607.

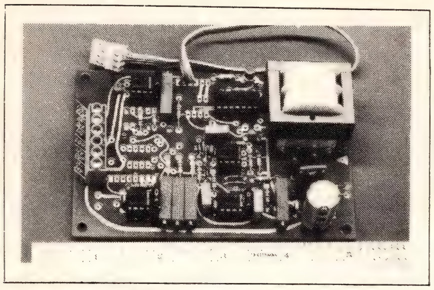
Circle No 365

FIBER-OPTIC LAN

The Codenet-3050 lets you develop a fiber-optic LAN for your IBM PC and compatible computers by attaching a Transceiver/Adapter to a PC Network adapter. No soldering or special tools are required. The system is compatible with all software written for the IBM PC Network and the NetBios interface. The unit comes in a standard model for network clusters of 16 PCs. A high-power model is available for network clusters of 64 PCs. Standard model, $495; advanced version, $750.

Codenoll Technology Corp, 1086 N Broadway, Yonkers, NY 10701. Phone (914) 965-6300. TLX 646159.

Circle No 366

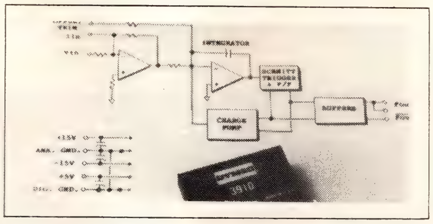


CONVERTER

The Interface Adapter, a current/voltage-to-frequency converter, allows you to utilize your phone lines or other communications systems for remote control of your control process. Output pulses can be either voltage source or current sink. You can use the adapter with any 4- to 20-mA, 0 to 5V, or 1 to 10V analog or sensor input. The adapter produces a frequency output that has ±0.1% linearity and repeatability. Output has offset and span adjustments for frequency outputs ranging from 0 to 50 Hz to 1000 to 10,000 Hz. The unit is transformer isolated from the ac power line for safety; it can also work with a dc source. From $58.

Automation for Industry Inc, Box 518, Littleton, MA 01460. Phone (617) 486-9416.

Circle No 367

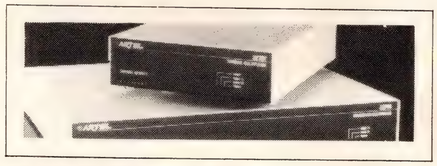


V/F CONVERTER

Featuring 0.05% linearity on a 10-MHz full-scale output frequency, the Model 3910 has nearly identical performance and characteristics of similar units costing as much as 40% more, according to the manufacturer. It provides complementary frequency outputs that will drive a 50-pF capacitative load. It accepts a −100 μV to −10V single-ended analog input signal. The temperature coefficients are 10 μV/°C for offset and 60 ppm/°C for gain. Power dissipation is 0.85W max. The converter is housed in a 1.31×0.69×0.22-in., 22-pin, double-width DIP. $78 (1000).

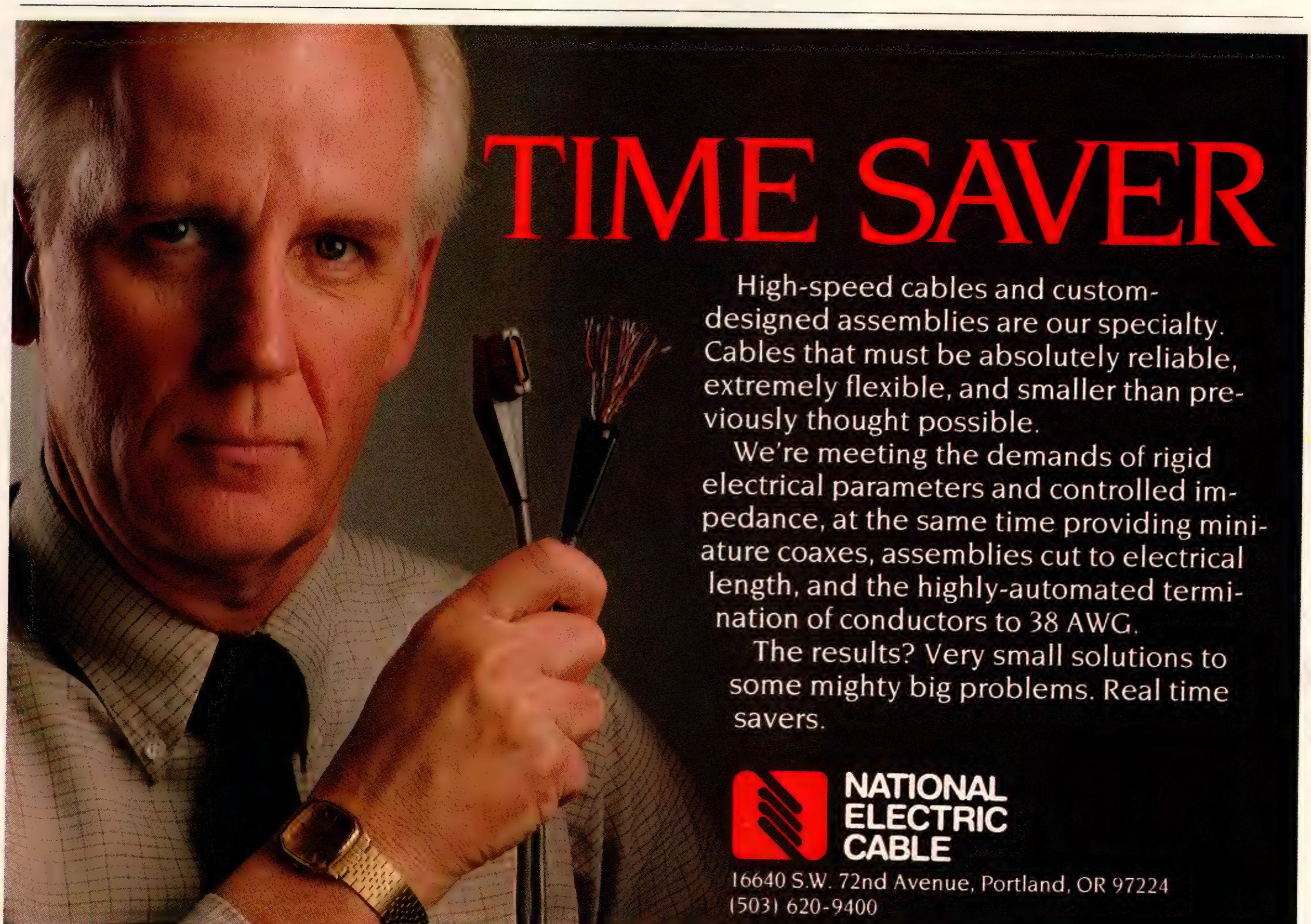
Dymec Inc, 8 Lowell Ave, Winchester, MA 01890. Phone (800) 225-1511; in MA, (617) 729-7870. TWX 710-348-6596.

Circle No 368



MULTIPLEXER

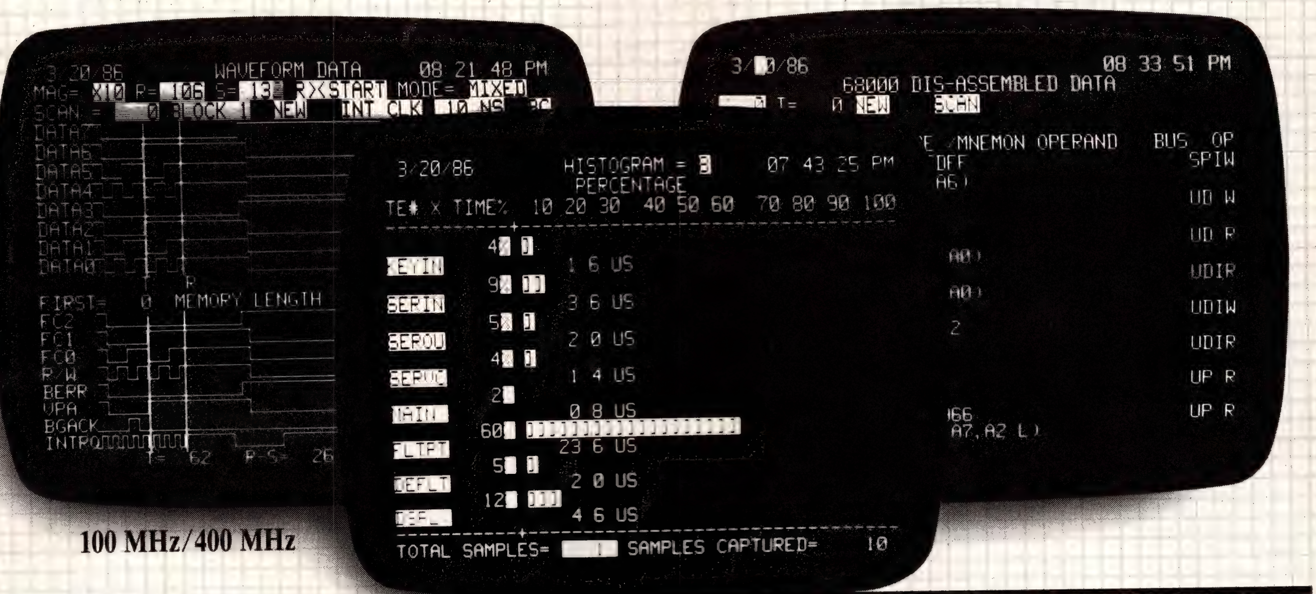
The Slimline multiplexer connects eight to 32 IBM 3270 Class A devices to a terminal multiplexer. An IBM 3274 controller connects as many as 32 ports to the unit. The



CIRCLE NO 142

Intech Model 2300 Logic Analyzer

Intech stands alone.



Only Intech offers Hardware to 400 MHz –Software to 125 MHz.

Hardware Analysis

Only the Intech Model 2300 Logic Analyzer gives you up to 64 channels at 100 MHz and 8 channels at 400 MHz. Glitch capture on all 64 channels. No more messy probe changes going from software recording to hardware recording. The Model 2300 stands alone as the world's premiere hardware Logic Analyzer!

Software Analysis

The Model 2300 has a powerful combination of software analysis features unrivaled by any other on the market. Time Alignment allows up to 4 blocks of 16 channels each to be clocked from different sources, and aligned in the state display according to time of occurrence. Histogram allows accurate viewing of system performance according to time spent in up to 8 user definable locations. Unique to Intech's Model 2300 is the ability to vary clock resolution automatically during software performance capture. Program areas with extreme length of running time can be effectively and accurately analyzed. 64 levels of "If Then Else" triggering, area tracing, sequence count, and much, much more. Nothing else comes close.

Microprocessor Analysis

Intech offers the broadest range of microprocessor support in the industry. Who else covers all the 8-bit and 16-bit devices, including the 80186, 80286, 68020 and 32032? And, remember with our unique hardware channel arrangement, you can trace code and look at timing simultaneously. No matter how you look at the 2300, no one else measures up!

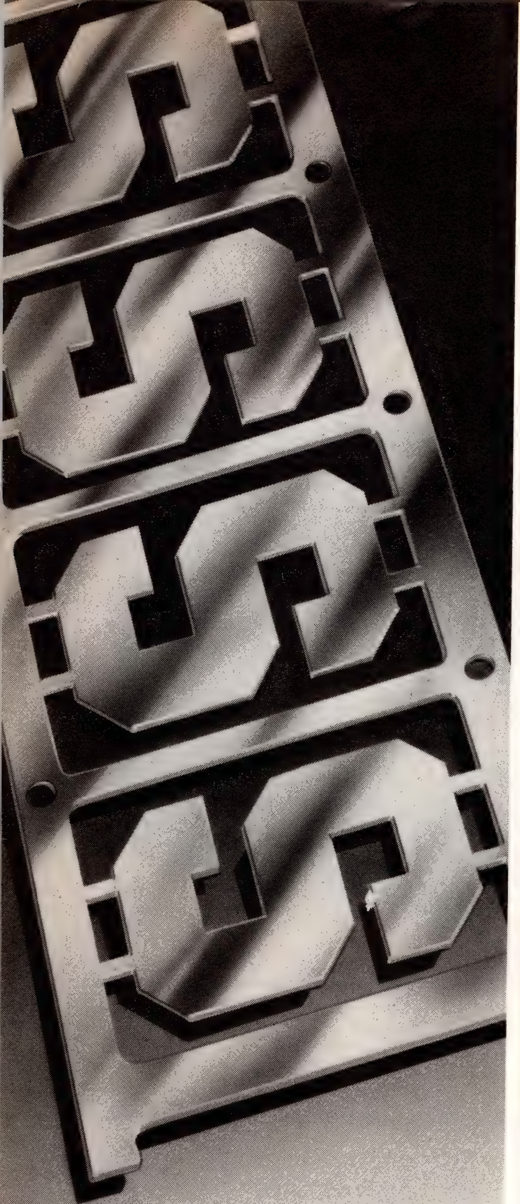
30 Out of Top 50 Buy Intech

That's right! 30 out of the top 50 electronic companies own Intech Logic Analyzers. Arrange a demonstration of the Model 2300 and you will understand why. There is nothing else like it!

For more information, write Intech Incorporated, Instruments Division, 282 Brokaw Road, Santa Clara, California 95050. Or call (408) 727-0500.

intech

CIRCLE NO 144



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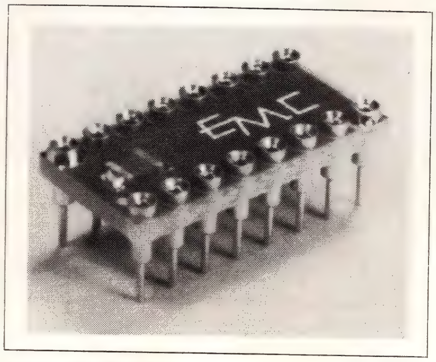
multiplexer then transfers data on one RG62-AU coaxial cable. The elimination of the multiple cables between controller and terminals greatly reduces duct crowding and stress, according to the manufacturer. You can use the multiplexers in point-to-point, multidrop, or star combinations. One 32-port MUX can communicate with as many as four terminal units at different points in a building. Stand-alone and rack-mount versions are available. $2000.

Artel Communications Corp, Box 100, West Side Station, Worcester, MA 01602. Phone (617) 752-5690.

Circle No 369



IC SOCKET

The Silencer combines a socket with a decoupling capacitor within the same physical area of standard sockets, thus saving board space. It is available in models with 6 to 48 positions and comes in a variety of terminal styles, including standard pc mount, low-profile pc mount, and wire wrap. Capacitor value can be 0.1, 0.01, or 0.33 μF (for 256k dynamic RAMs). The capacitor has no leads and is surface mounted on 0.062-in.-thick, copper-clad glass epoxy laminate. It is located adjacent to the V_{CC} pin and connects via a small circuit trace. The ground connection is actually a ground plane that partially encircles each pin location and then connects (via a solder pad) with the ground pin location. This design provides an additional shield from noise. A 16-pin unit with pc-mount pin, plated with gold or tin, $2.24 (100). Delivery, three to six weeks ARO.

Electronic Molding Corp, 96 Mill St, Woonsocket, RI 02895. Phone (401) 769-3800. TWX 710-387-1350.

Circle No 370

S/H MODULES

The ZSH281 S/H module provides feedthrough of −96 dB and a dielectric absorption of 0.002% per change in input step, allowing acquisition to 16-bit accuracy. It features a 3-μsec max full-scale acquisition and settling time. The companion ZSH280 module offers a 1-μsec settling time to 0.01% and an input impedance of $10^8 \Omega$. ZSH281, $120; ZSH280, $134.

Analog Solutions, 940 Detroit Ave, Concord, CA 94518. Phone (415) 686-6660.

Circle No 371

DIGITAL CONTROLLER

The DTC-451 digital transducer controller is a single-channel instrument for the excitation and readout of ac-operated LVDT-type transducers. The unit has a digital display and dual set-point analog limits with indicator lights. You can adjust limits on the front panel; other ad-

An end to power surges from the power in wiring devices.

Back in 1888, when Harvey Hubbell invented the pull chain light socket, nobody worried about power surges.

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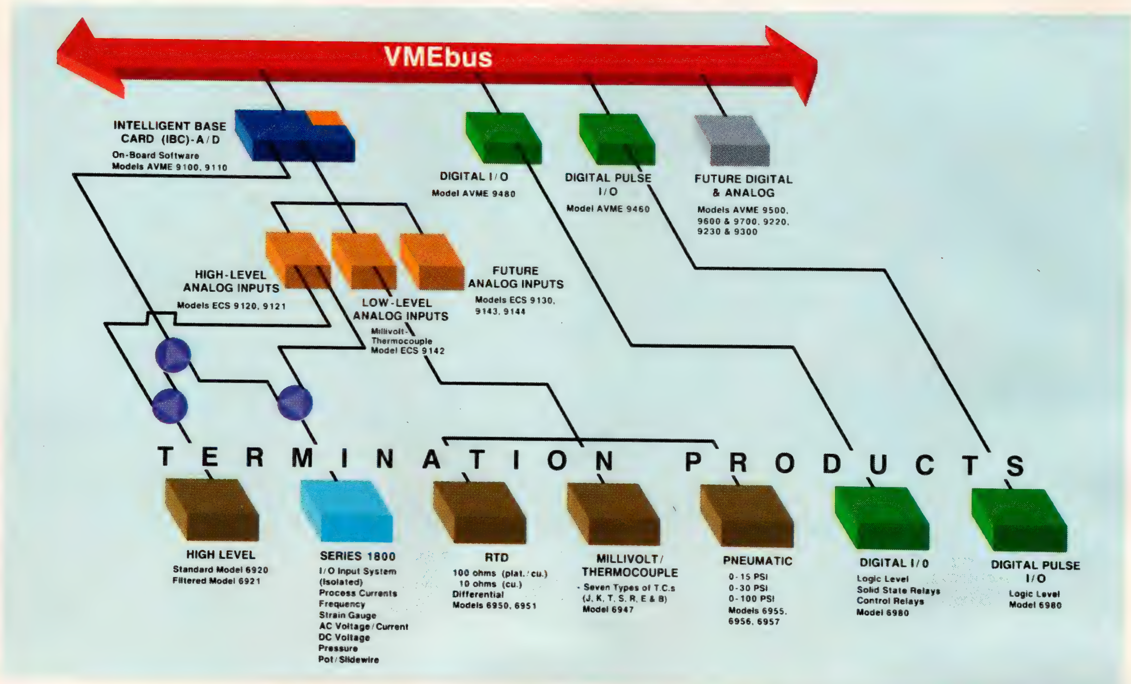
Maybe that's why, after nearly a century of innovations, we're still the power in wiring devices.

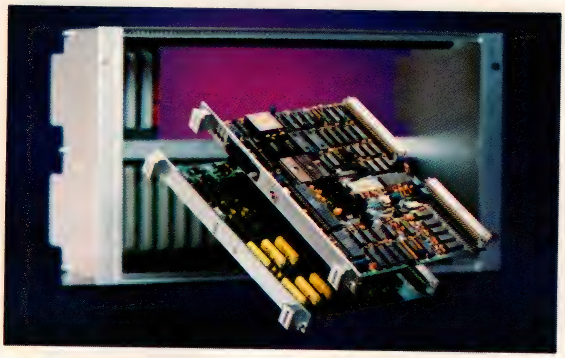
CIRCLE NO 146

EASY AS IBC

Advanced VME industrial I/O capability



VME-Industrial I/O signal interfacing is now a simple matter of "putting it on the bus." Thanks to Acromag's analog and digital cards and termination products for interfacing real world I/O signals.

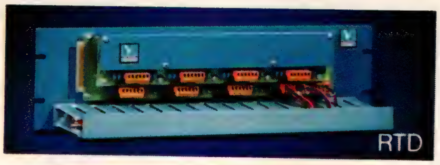


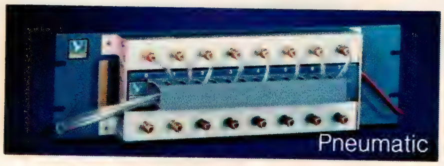
Field inputs such as thermocouple, RTD, voltage, frequency, strain gauge, pneumatic and many others are directly interfaced via screw type termination products and I/O cards to the VMEbus—as easy as IBC.

The Analog Intelligent Base Card (IBC) simplifies the problem by forming an intelligent base for the analog subsystem collecting and conditioning up to 256 analog signals and storing all in dual port RAM memory. The IBC and analog I/O cards provide for 14-bit A/D conversion, amplification, isolation, scaling, linearization and limit checking. The IBC card also has a local serial port for calibration, diagnostics and configuration.

And digital I/O? Of course... provided for by a 64 channel 30 volt bi-directional I/O card with or without relay field interfaces using a variety of screw type termination panels.

Acromag's VME cards and termination products provide the broadest industrial I/O capability available. All to make solutions to your industrial I/O needs as easy as IBC.





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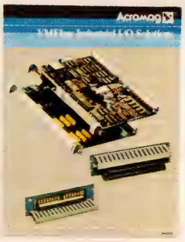
To find out more about Acromag's VME Industrial I/O capability and commitment write for Bulletin 20-000.0. Or for immediate help call our telemarketing department at 1-800-ACROMAG or (313) 624-1541.



CIRCLE NO 147

justments, such as span, phase, and range of zero (30 or 100% full scale) are performed with externally located controls. The set-point range is ±100% full-scale output; set-point repeatability is ±0.01% of full-scale output; set-point hysteresis is internally adjustable at 0 to 10% of full-scale output. Excitation frequency is also user selectable at 2.5 kHz or at 10 kHz. Constant voltage excitation, adjustable from 1 to 5V rms, is convertible to constant current excitation. Three-state parallel BCD output is optional. $995.

Schaevitz Engineering, Box 505, Camden, NJ 08101. Phone (609) 662-8000. TWX 710-892-0714.

Circle No 372

CONNECTORS

With a profile of <0.4 in. from the pc board to terminations, the Series 200 connectors feature fully shielded replaceable contacts. Designed primarily for use in high-density packaged electronic assemblies, the connectors can be ordered in either single-row format with two to 17 positions in seven sizes or two rows with four to 34 positions in 11 sizes. Male connectors have either straight or 90° terminations compatible with pc boards of 0.05 in. nominal thickness. Female connectors can be terminated by either crimp or soldering with crimp models available in two sizes of crimp contacts. Other female-connector options consisting of straight pc-tail contacts are available for applications requiring both rigid and flexible printed circuits. $0.50 to $15. Delivery, 4 to 12 weeks ARO.

McMurdo Connectors, Box 248, Lexington, MA 02173. Phone (617) 863-8898.

Circle No 373

DIGITAL ENCODER

The HEDS-9000 Series optical incremental encoder consists of a lensed LED emitter and a detector IC enclosed in a C-shaped plastic package. When operated with a code wheel, the module translates the rotary motion of a shaft into a 2-channel digital quadrature output. By choosing a code wheel and the

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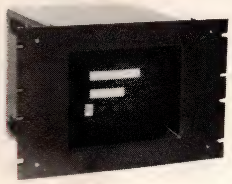
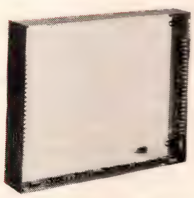
Desktop TID



Rack-mount TID



Custom Touch Panel

Coming Soon: Color Touch and Flat TID

The **Touch Information Display** (TID) functions as a standard ASCII terminal or PC compatible monitor. Both are available in a rugged metal desktop or rack-mount housing, suitable for both public and industrial environments.

The 12″ monochrome **TID Terminal** and **Monitor** communicate through an RS-232 or optional RS-422 port. (Monitor accepts RS-170 composite video input) With the Terminal, an optional feature is 16 pages of downloadable display memory.

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CIRCLE NO 148

96 reasons to choose NEC chip tantalum caps.

NEC gives you a choice of 96 different tantalum chip capacitor types. Our R-Series offers capacitance values ranging from 0.01 to 68μF. And voltage ratings from 4 to 35VDC.

NEC's R-Series capacitors come in bulk, magazine, stick and standard tape supply formats. Their surface mount packages offer dramatic space savings. They're reeled on standard 8 or 12mm tape to save time with automatic placement. They're 100% burned-in to minimize reliability problems. And specially designed to withstand the stress of dip and reflow soldering.

As the world leader in precision molded chip tantalum capacitors, NEC has the capacity to meet your system needs. 96 ways.

μF \ V	4	6.3	10	16	20	25	35
0.01							A
0.015							A
0.022							A
0.033							A
0.047							A
0.068							A
0.1							A
0.15							A
0.22							A
0.33						A	A
0.47					A	A	B•B2
0.68				A	A		B•B2
1			A	A			B•B2
1.5		A	A	A		B•B2	C
2.2	A	A	A	B	B•B2		C
3.3	A	A	B	B•B2		C	C•D
4.7	A	B	B•B2	C	C	C	D•D2
6.8	B	B•B2	C	C	C	D•D2	D•D2
10	B•B2	C	C	C•D	D2	D•D2	
15	C	C	C•D	D2	D•D2		
22	C	C	D•D2	D•D2			
33	C	D•D2	D•D2				
47	D•D2	D•D2					
68	D•D2						

	W	L	H
A case	1.6 (.063)	3.2 (.126)	1.6 (.063)
B2 case	2.8 (.110)	3.5 (.138)	1.9 (.075)
B case	2.6 (.102)	4.7 (.185)	2.1 (.083)
C case	3.2 (.126)	6.0 (.236)	2.5 (.098)
D case	4.3 (.169)	7.3 (.287)	2.8 (.110)
D2 case	4.6 (.181)	5.8 (.228)	3.2 (.126)

mm (inch)

For further information, please contact:

USA	**NEC Electronics Inc.** **Tel:415-960-6000. TWX:910-379-6985**
Europe	**NEC Electronics (Germany) GmbH** **Tel:0211-650302. Telex:8589960 NE D.**
	NEC Electronics (Benelux) **Netherlands** **Tel:040-445-845. Telex:51923 NEC B NL.**
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Computers and Communications

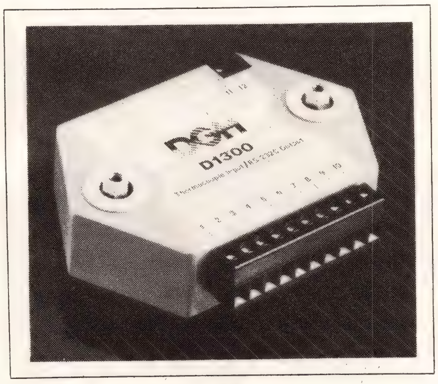
CIRCLE NO 149

NEC

external housing, you can customize the encoder. Although designed to operate with the HEDS-5100 and -6100 Series code wheels, you can use your own code wheel if you prefer. Standard resolutions of 360, 500, and 1000 counts per revolution are available. The quadrature states of the encoder typically vary no more than five electrical degrees. The quadrature signal is guaranteed over −40 to +100°C and a frequency range to 100 kHz. The module is TTL compatible and operates from one 5V supply. $20.50 (250).

Hewlett-Packard, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 374



A/D MODULES

The D1000 Series analog/digital modules combine analog-input-signal conditioning and A/D conversion; they communicate, in ACSII, over an RS-232C or RS-485 link. The family has 42 models featuring the following variables: voltage (±100 mV, ±1V, ±5V, ±10V dc); current (±10 mA, ±100 mA, ±1A); thermocouples (J, K, T, E, R, B, C); 100Ω resistance-temperature detector; bridge (±30; ±100 mV); frequency or pulse (10 Hz to 20 kHz; 100 μsec to 100 sec); and digital (seven inputs and eight outputs). The thermocouple module amplifies a 1-μV input signal, compensates for cold junction, linearizes the output, and scales it in °C or °F. Conversion rate is 10/sec. Input burnout protection is 250V ac. Measurement resolution is 1 part/50,000. Every module has digital input/output lines for on/off control that use solid-state relays or TTL signals. An 8-bit μC performs all scaling, linearization, and calibration tasks in software, eliminating the need for pots, switches, or adjustment hardware. Each module requires a 10 to 30V dc unregulated supply at 0.7W max. Rated performance is specified from 0 to 70°C, but the modules will operate from −25 to +85°C. $250 or $325. Delivery, 8 to 10 weeks ARO.

DGH Corp, Box 5638, Manchester, NH 03108. Phone (603) 622-0452.

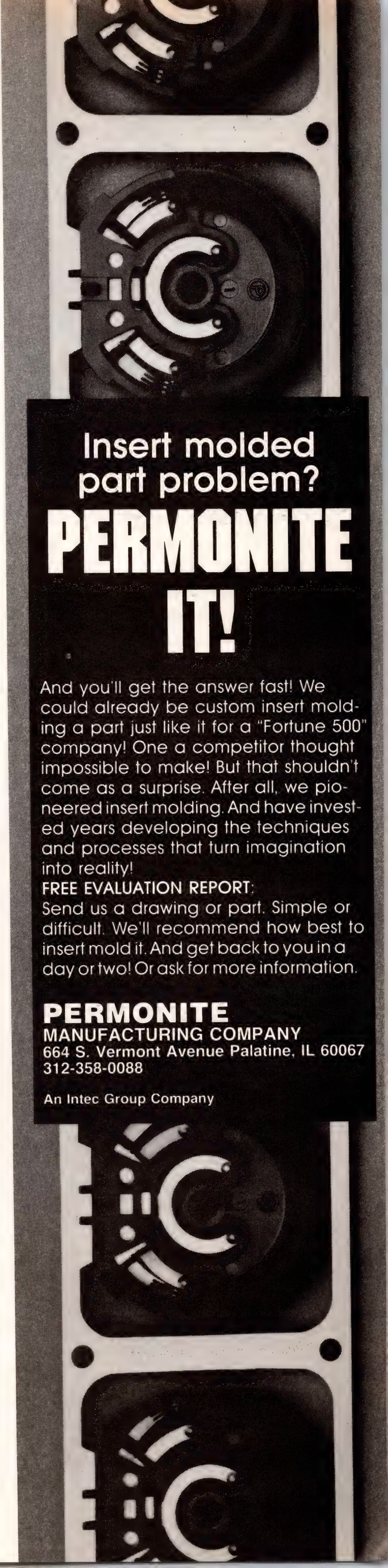
Circle No 375

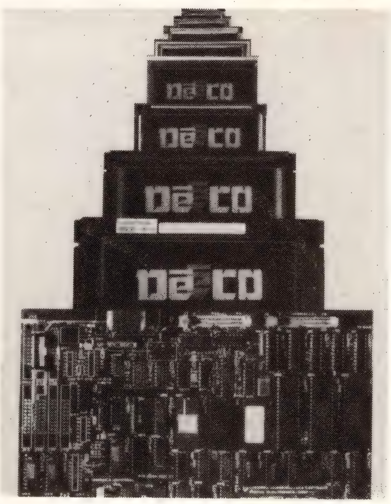
SYSTEM CHASSIS

This 12-slot Multibus I industrial enclosure, the Microbox MBI-12, is constructed out of 16-gauge steel. Compartments for two 5¼-in. half-height storage units are located underneath the card rack. You can mount additional storage units or auxiliary power supplies in an open area behind the card rack. The chassis comes with a 235W switching power supply that provides 5V at 35A, 12V at 4A, −12V at 1.5A, and −5V at 1.5A. In addition, a 400W switching power supply furnishing 5V at 50A is available. Three industrial equipment fans cool the card rack and the power-supply area. Features include a front-panel power-status display, removable key switch with off, on, and reset positions, and a system-run and -halt indicator. The back of the enclosure has a circuit breaker, a dual 115V outlet, four DB-25 serial I/O connectors (with four additional mounting holes for DB-25 connectors), and two rectangular slots for ribbon-cable access. A removable rear panel gives you access to both the power supply and any additional drives. $1845.

Key Designs, 20 N Clark St, Suite #610, Chicago, IL 60602. Phone (312) 263-1618.

Circle No 376



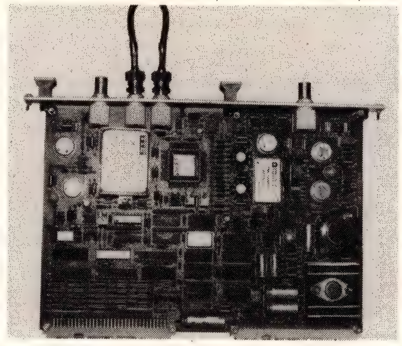


GRAPHICS CONTROLLERS

The C2 Series controllers interface with electroluminescent and gas-plasma dot-matrix flat-panel displays, including the 512×256-dot panels from Planar, Lohja, Sharp, and NEC. They can control displays with matrices having as many as 512×512 dots. The controllers have both 8088 and NEC7220 processors that provide a dual-pipelined architecture. Either 8-bit parallel or serial (RS-232C or RS-449) host interfaces are available. An IBM PC-style keyboard is standard; a touch-panel interface is optional. You can store 2k bytes of user-defined characters and as much as 6k bytes of locally retained graphics segments in an optional EEPROM. The controllers' software implements all the virtual device interface (VDI) standard commands and many other high-level commands, including several touch-screen commands, character zoom (16 levels), paint commands, multiwindowing, and trace commands. The controllers operate on a 5V power supply. $895 (100).

Digital Electronics Corp, 26142 Eden Landing Rd, Hayward, CA 94545. Phone (415) 786-0520. TLX 172073.

Circle No 377



A/D CONVERTER

The AD8/50M A/D converter is a single-board system with a sample rate as high as 50 MHz and 8-bit accuracy. A ±0.5V-input amplifier and a track-and-hold circuit feed the input samples to the board's flash A/D converter. The combination provides 8-bit accuracy at 20 MHz. The overall analog front-end gain demonstrates <3-dB rolloff at 25 MHz. Software-controlled logic-output buffers allow you to disconnect the output and substitute a voltage

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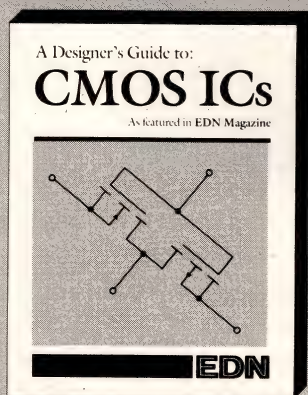

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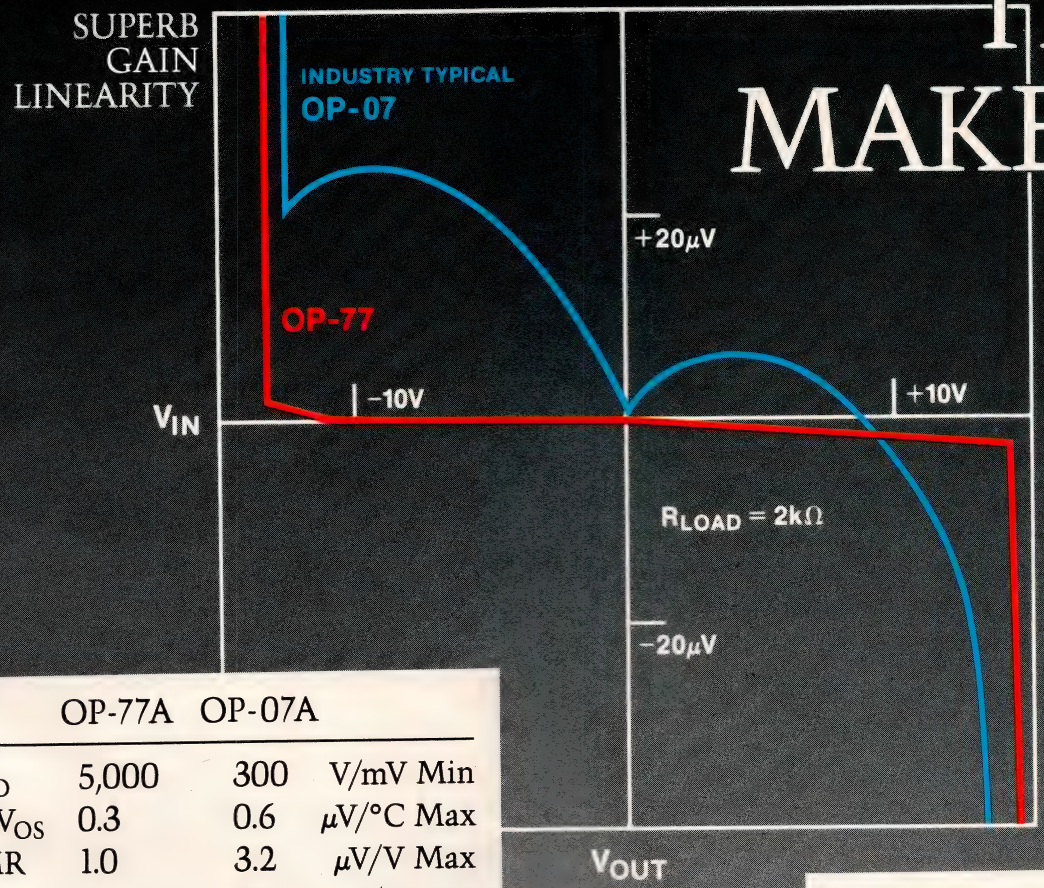

	OP-77A	OP-07A	
AV_O	5,000	300	V/mV Min
TCV_{OS}	0.3	0.6	μV/°C Max
CMR	1.0	3.2	μV/V Max
PSR	3.0	10.0	μV/V Max
P_D	60	120	mW Max

OP-77 obsoletes OP-07.

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A Bourns Company
1500 Space Park Drive
Santa Clara, CA
95054-3499
(408) 727-9222

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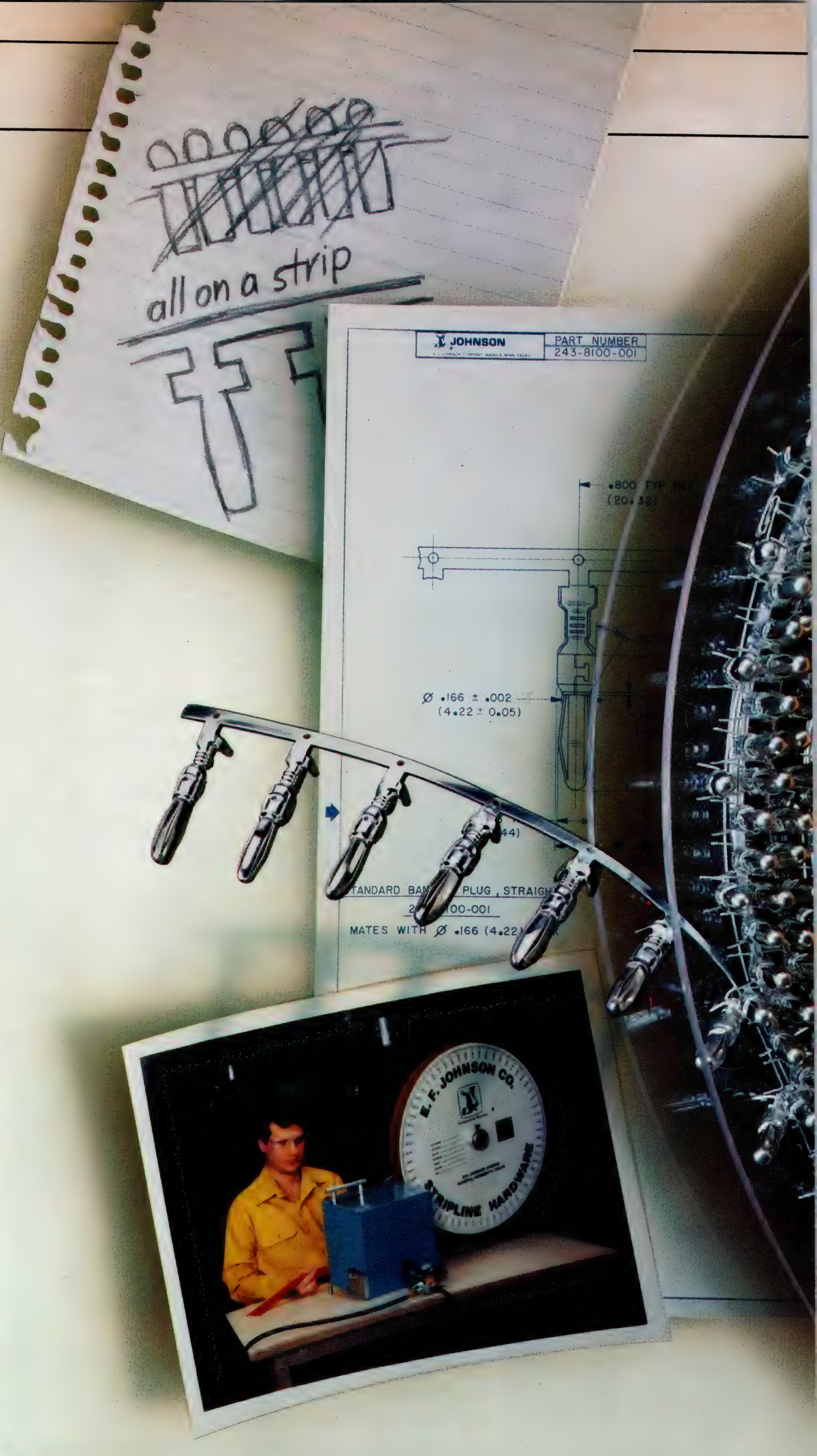

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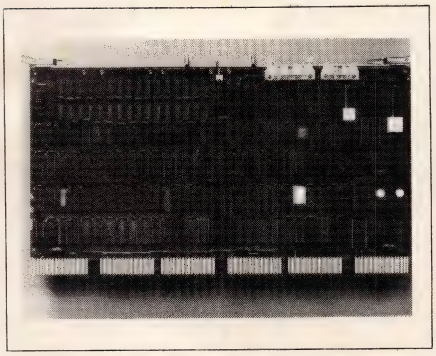
equal to +½ full scale; or it allows you to substitute a ramp that ranges between ± full-scale voltage. If your application requires an external clock, you can disconnect the converter's internal master oscillator. You use jumpers to divide the clock input by 2, 4, or 6; under software control, clocks can be further divided by 2, 4, 8, or 16. Although the board is VME size, it does not conform to the VME Bus data formats because its data rates are above VME capabilities. DC-voltage requirements are ±15, −5.2, and 5V; power dissipation is about 15W. $7000. Delivery, stock to six weeks ARO.

DSP Systems Corp, 1081 N Shepard St, M/S-E, Anaheim, CA 92806. Phone (714) 630-1330.

Circle No 378



VAX-LAN BOARD

The Ivecs (integrated VAX Ethernet communications server) plugs into one hex-size Unibus slot in a VAX, emulates as many as eight of DEC's DMF 32 I/O controller cards, and thereby establishes a direct attachment to an Ethernet LAN. The server allows network connections to the VAX for as many as 64 devices attached to the LAN. Included in the server package are a 12-MHz 68000 CPU, an AMD Lance Ethernet controller chip, 1M byte of RAM, and the DMF 32 interface. This server takes the place of multiple DZ/DH or DMF I/O cards inside the VAX host. The server's emulation provides both Silo and DMA modes with terminal support as well as host file-transfer operation across the Unibus interface. The unit can transfer multiple characters on a single Unibus interrupt. $6900; per port connection, $108; annual software license fee, $250.

Bridge Communications Inc, 2081 Stierlin Rd, Mountain View, CA 94043. Phone (415) 969-4400. TLX 176544.

Circle No 379

GRAPHICS PROCESSOR

The XP/48, a graphics extension processor, attaches to an IBM PC, PC/XT, PC/AT, or compatible with a parallel interface, and it turns the computer into a 48-bit, virtual-memory, device-independent graphics computer. You can create graphics on the system or enter them into it. You can then merge,

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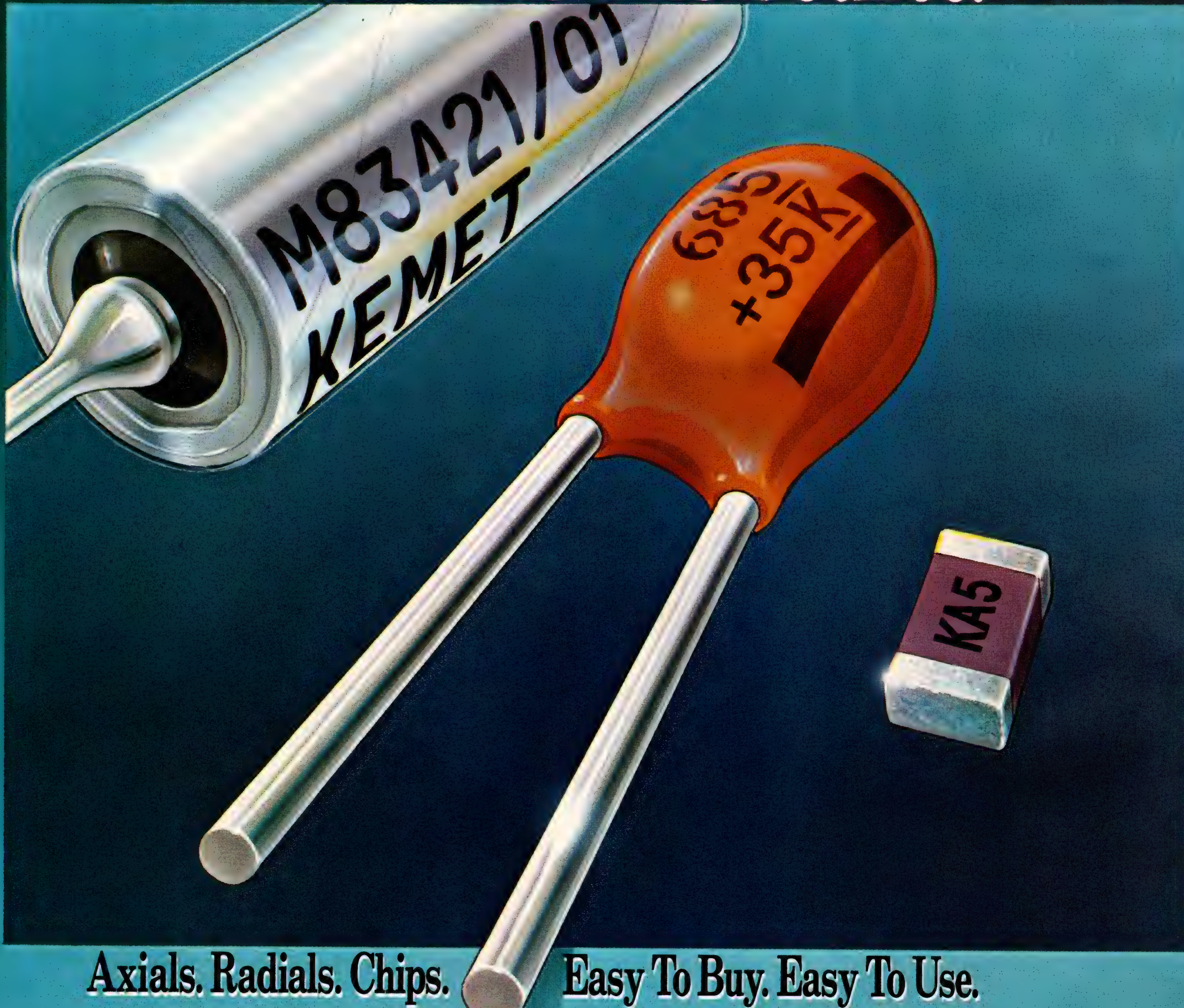

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CIRCLE NO 154

edit, and manipulate graphics and transmit the image for printing. You can also generate color separations that produce four B&W images for process color printing. The system can work with 16.7M colors simultaneously and can drive any combination of more than 100 hard-copy devices. The graphics software packages it runs include a command file interpreter and a library of more than 40 type fonts. You can enter graphics from a digitizing pad with pen or mouse, a standard video camera, or one of a variety of scanners, including an Eikonix color scanner with resolution as high as 4096×4096 pixels. All PC programs, regardless of their source language (C, Pascal, Fortran, etc), can transmit graphics to the processor. Standard features include a 48-bit, (TTL-bit-slice) virtual-memory processor, 393k bytes of main memory, and a 20M-byte internal fixed disk. Hardware options include four serial ports, a GPIB port, a function processor and graphics accelerator, a video processor, a 1530×1180-pixel color-graphics monitor, a ½-in. magnetic-tape interface, additional main memory, and additional fixed-disk storage to 80M bytes. From $12,500.

Superset Inc, 11025 Roselle St, San Diego, CA 92121. Phone (619) 452-8665.

Circle No 380

PC-GRAPHICS LINK

The Viking 1 graphics subsystem for the IBM PC/AT, PC/XT, RT PC, and compatibles drives 1280×960-pixel graphics programs and 24×80-character text on a single 19-in. monochrome monitor. It has a 1024×2048-bit video memory of which 1280×960 bits are displayed, thereby leaving the 768×1024-bit section of nondisplayed memory available for font and format storage. Its controller uses the Hitachi HD63484 ACRTC graphics control chip and a DMA

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Raytheon's TDU-850, Thermal Display Unit, produces photo quality images on an 8¾" x 200 ft. roll. The TDU-850 prints 16 shades of grey in less than 20 milliseconds per line; black and white images at 5 milliseconds per line. Price per unit from $4950, depending on interface and application. (Slightly higher overseas). Discounts for OEM large volume quantities. Fixed thermal head assures perfect registration. Resolution better than 200 dots/inch. Direct thermal technology requires no toners or developers. Standard or custom interfacing. For details, contact **Marketing Department, Raytheon Ocean Systems Company, Westminster Park, East Providence, RI 02914 USA. Telephone (401) 438-1780 Telex 6814078.**

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controller. Using a 10×16-bit character cell, the hardware character generator provides 60 128-character lines of alphanumeric data. The generator can operate concurrently with the graphics memory. $2195.

Moniterm Corp, 5740 Green Circle Dr, Minnetonka, MN 55343. Phone (612) 935-4151.

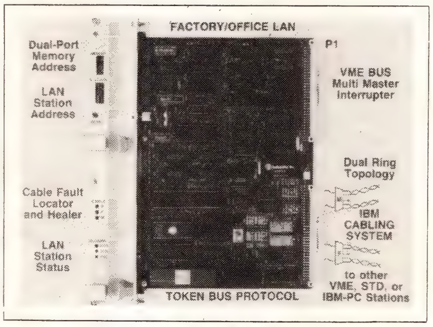
Circle No 381

REAL-TIME CPU

Operating at 12.5-, 16.5-, or 20-MHz clock rates, the CPU-4RT VME Bus CPU board provides as much as 128k bytes of EPROM and offers an optional MC68881 floating-point coprocessor. The assembly offers a zero-wait-state memory at 16.5- and 20-MHz clock rates. The company configures 256k-byte, 1M-byte, or 4M-byte versions of onboard, dual-ported memory. The board's I/O section features the 68561 MPCC IC for transmissions as fast as 4M bytes/sec and the MC68681 DUART IC for two additional serial ports. $2000 to $2500.

Electronic Modular Systems Inc, 4546 Beltway, Dallas, TX 75244. Phone (214) 392-3473.

Circle No 382



VME LAN BOARD

The NETPC/VME LAN board, a member of the token bus family, uses carrier band data transmission over the IBM Cabling System and features a 68008 CPU, resident firmware, and a WD2840 LAN controller. Together these devices provide all network functions through the ISO transport level. A LAN board directly supports multiple VME Bus Masters; multiple-message buffers are provided in dual-port RAM. The network software allows onboard logic to locate and bypass any single cable or station fault by automatically reconfiguring to a fully connected daisy-chain topology. To maintain an adequate signal-to-noise ratio, each station reamplifies the LAN signals while differential receivers and optical isolation provide common-mode noise rejection. These operations allow 300m cable lengths between adjacent stations, and the complete system can extend more than 5 km. This board supports STD Bus and IBM PC bus computers. $1795.

Beal Communications, 9794 Forest Lane, Suite 246, Dallas, TX 75243. Phone (214) 340-2044.

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True Full Speed Emulation Now Available With Overlay Ram!

The I.C.E.BOX is a small, compact emulator, easy to move and use. Though it costs about the same as other handheld emulators, it is the only portable unit that offers true full speed emulation with hardware breakpoints. The I.C.E.BOX has 65,535 hardware breakpoints that can be set anywhere in memory—even in ROM! Optional ICEpack software supports symbolic debugging and includes ICEBASIC, a BASIC language designed especially for use with the I.C.E.BOX. Use it to create custom automation packages for production test and service. And now the REFRIGERATOR is available to tackle your toughest debugging jobs. The REFRIGERATOR is an I.C.E.BOX with the bonus of 16K of overlay RAM. The REFRIGERATOR can downlaod code into your target system's ROM address space!

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The I.C.E.BOX is available for the Z80, 8085, and NSC800 processors for $600.00. The REFRIGERATOR (Z80 only) is $900.00. Contact Softaid, Inc., 8930 Route 108, Columbia, MD 21045 — (301) 964-8455. We accept Visa, Mastercard, checks and COD.

SOFTAID, Inc.

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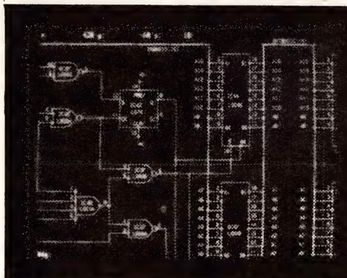

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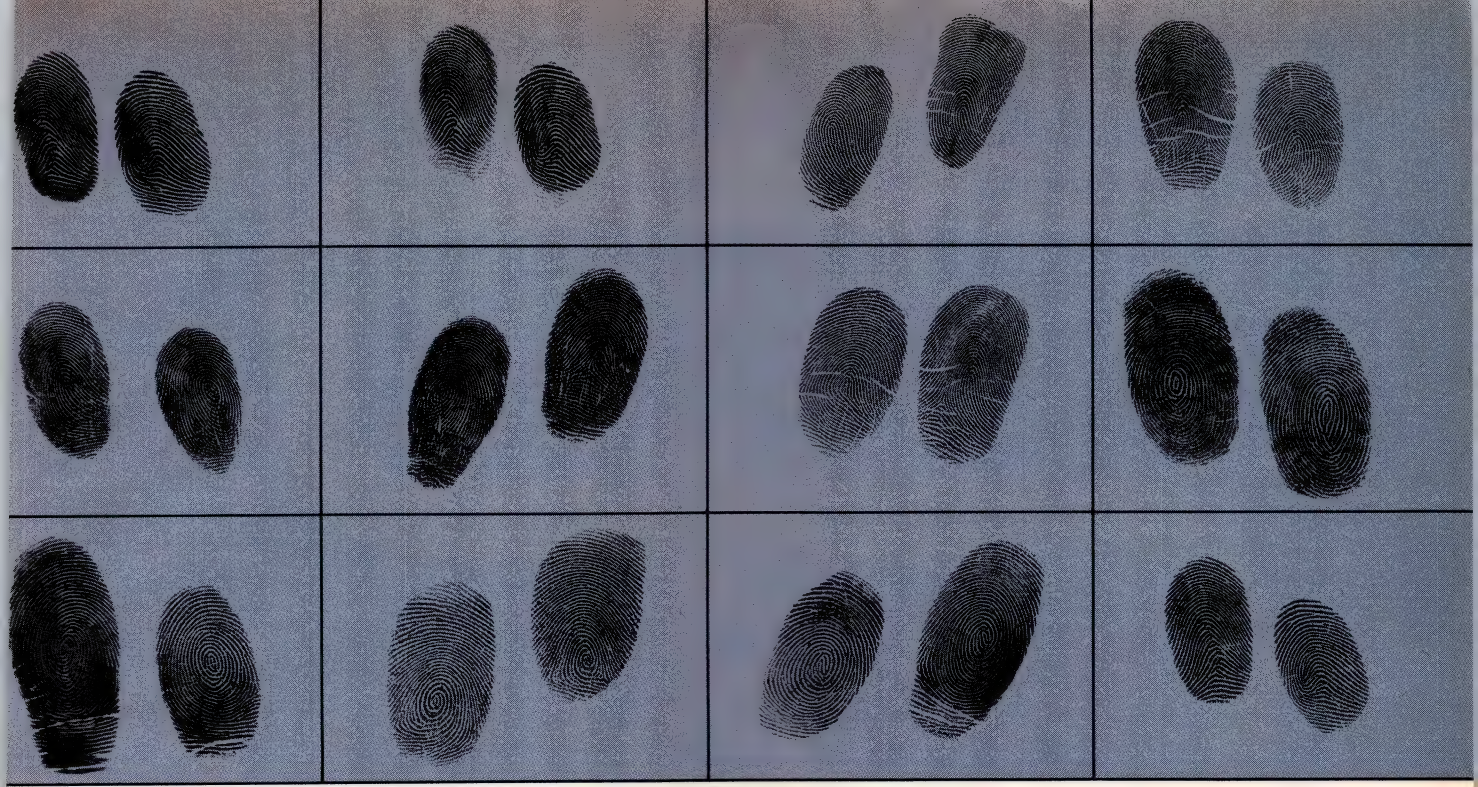

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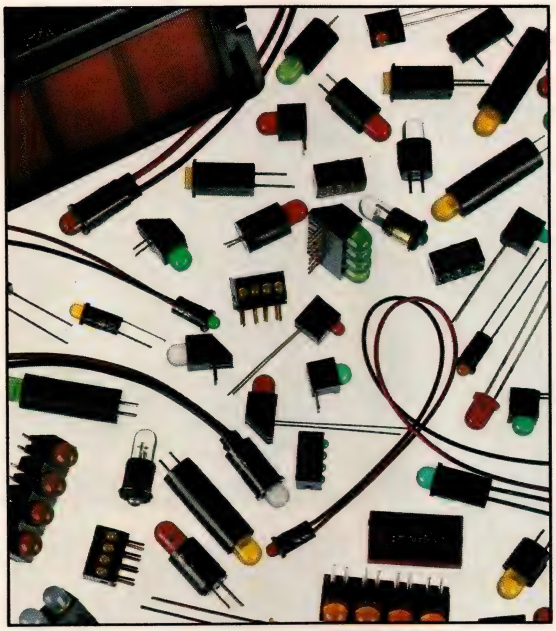

With everything electronic getting smaller, PC boards and front panels are getting more complicated and difficult to service.

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Suppose you want to backlight a front panel from an internal PC board.

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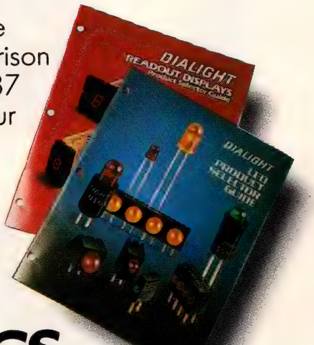

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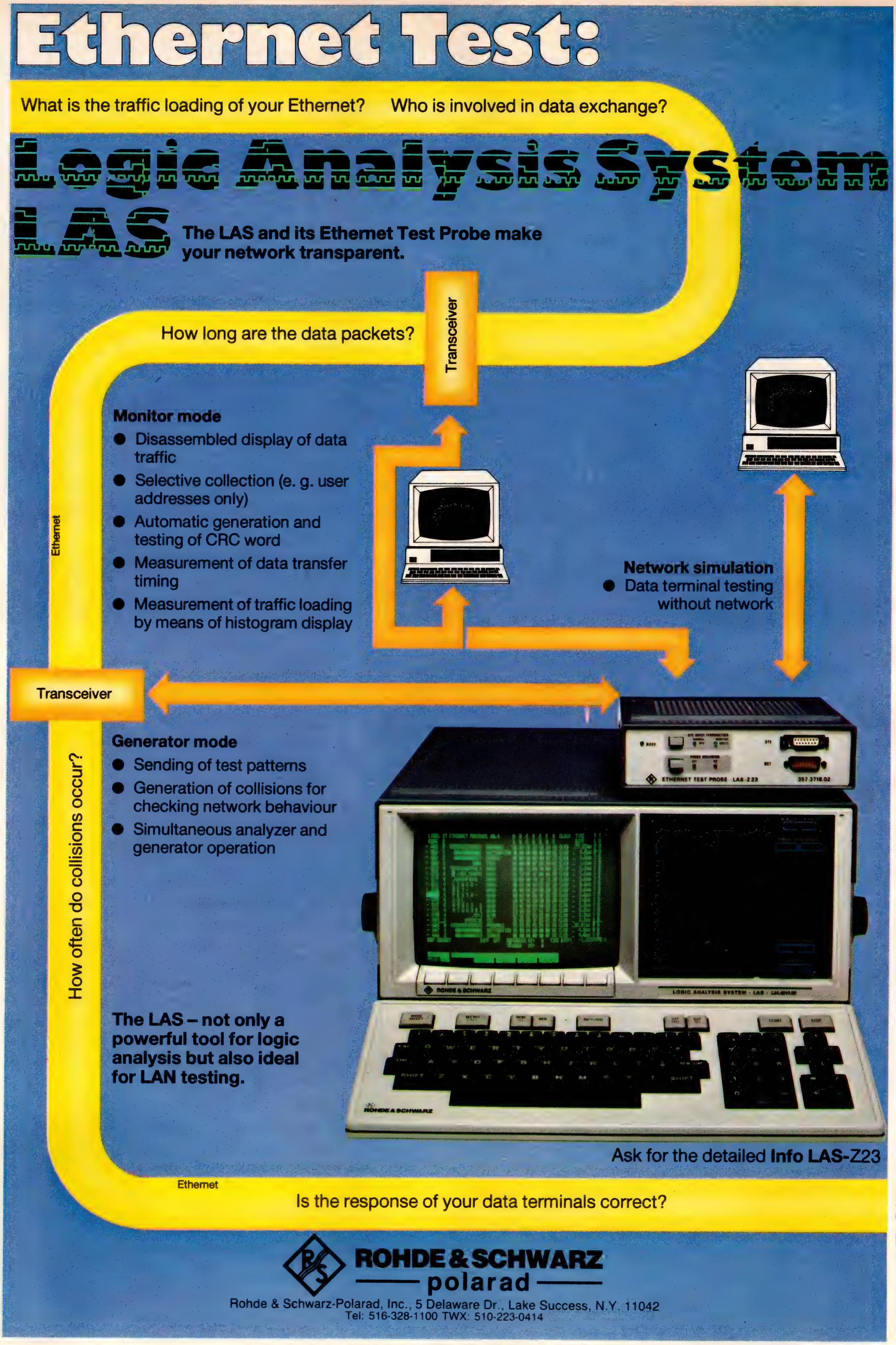
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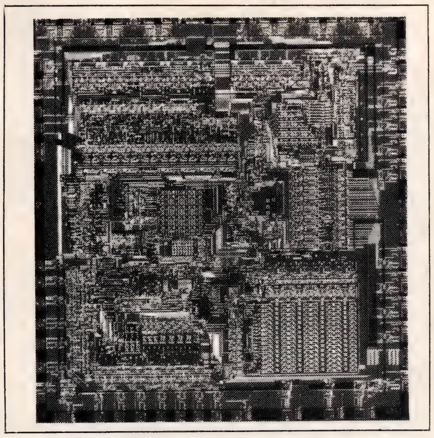

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The Am29X305A 8-bit μC offers a 200-nsec cycle time. The device can fetch, decode, and execute 16-bit instructions in one machine cycle. It provides high-data throughput with both bit- and byte-oriented operations and replaces 50 medium-scale integrated circuits. It features on-chip registers and data-handling capability as well as separate data buses for instruction, instruction address, and 3-state I/O functions. Thirteen 8-bit, general-purpose working registers enhance the data-handling capabilities of the μC. Within one instruction cycle, you can program the 8-bit data-processing path to rotate, mask, shift, or merge single or multiple subfields. In a ceramic DIP, $29.70 (100).

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

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The FDC9238 is a high-resolution data-separator chip designed for use with floppy-disk drives. The device is compatible with 3½-, 5¼-, and 8-in. floppy-disk drives. The device uses a 16-bit cell-divide algorithm, which yields significant improvements in soft-error rates over existing designs. An internal crystal oscillator and clock generator provide the signals necessary to interface to a standard floppy-disk controller. In plastic and ceramic 14-pin DIP, $9.40 (100). Delivery, six to eight weeks ARO.

Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11788. Phone (516) 273-3100. TWX 510-227-8898.

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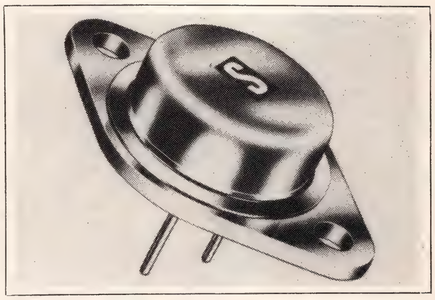

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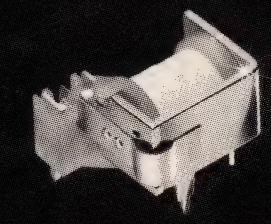

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emitter saturation voltage, and fast switching times. The npn versions come with ratings of 100, 120, 140 and 150V; pnp versions have ratings of 80, 100, and 120V. In TO-3 cases, npn types, $4.50; pnp types, $5.25 (100). Delivery, six to eight weeks ARO.

Solitron Devices Inc, 1177 Blue Heron Blvd, Riviera Beach, FL 33404. Phone (305) 848-4311. TWX 510-951-7610.

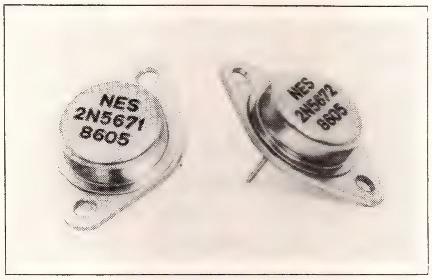
Circle No 386

MULTIPLIERS

The 2516 and 2010B are high-speed 16-bit multipliers. The 2516C is a 16×16-bit integer multiplier that operates at 38 nsec. The 2010B multiplier/accumulator operates at 45 nsec. The devices are fabricated with a 1.2-μm double-metal CMOS process. Applications for these devices are primarily in the digital-signal-processing market, specifically in digital filtering, fast Fourier transforms, array processors, and dedicated hard-wired digital signal processors. 2516C, $100; 2010B, $149 (100). Delivery, eight weeks ARO.

Weitek Corp, 1060 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 738-8400.

Circle No 387



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The 2N5671 and 2N5672 140W high-speed power switches can turn 15A of collector current on and off in 0.5 and 2.0 μsec, respectively. Collector current is 30A max, and the beta range is 20 to 100. Sustaining V_{CEO} is 120V. The transistors are fabricated with a double-epitaxial process and incorporate ultrasonically bonded leads. Less than $6 (100).

New England Semiconductor, 202 Boston Rd, North Billerica, MA 01862. Phone (800) 446-1158; in MA, (617) 663-5417. TLX 820123.

Circle No 388

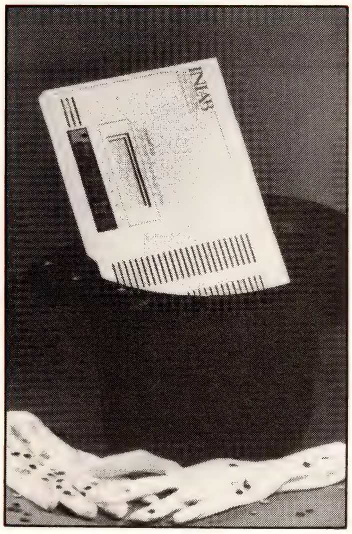
MICROCOMPUTERS

The μPD78310 and μPD78312 single-chip CMOS μCs feature on-chip memory, timers, I/O lines, A/D converters, multiple register banks, and an interrupt-handling facility, including microcoded macroservice channels. The CPU has as many as eight banks of registers. The memory access and I/O paths are 8 bits wide. Onboard program memory is 8k bytes of ROM, and data memory is 256 bytes of RAM. The μPD78310

CIRCLE NO 163

CIRCLE NO 201

MAGIC



THE INLAB 28
LOGIC/MEMORY
PROGRAMMER

It *must* be magic! How else could INLAB load all these features into such a small package:

- Capable of programming hundreds of logic and memory devices, including all of the most frequently used PLDs!
- Small and portable–less than 26 ounces!
- Completely software driven–ZIF Universal socket accepts all devices up to 28 pins!
- Available with CUPL™, the design software from Assisted Technology!
- Compatible with both JEDEC and Intel HEX download file formats!
- Standard RS232 interface links the Model 28 with most host systems!
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What more could there be? How about EPROM programming and emulation, from 2716 up to 27256 (including CMOS)? Its like getting an EPROM programmer/emulator–for free!

It's no illusion! For only $1995. we can make a Model 28 appear before your very eyes! Just give us a call at:
303/460-0103

We'd like to do some *magic* for you!

INLAB INC
A Hathaway Company
2150-I West 6th Avenue
Broomfield, CO 80020

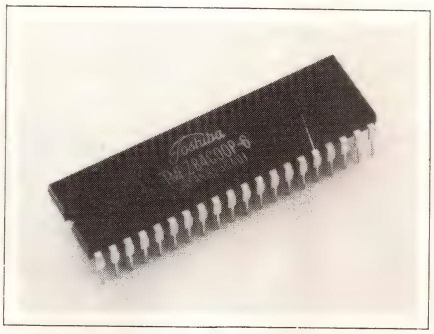
CUPL is a trademark of Assisted Technology; some elements of the Model 28 are manufactured and marketed under license from Digital Media, Inc.

CIRCLE NO 166

has no ROM, but both devices have a 64k-byte total address space. Input frequency is 12 MHz max. A 2-phase internal processor clock allows a 6-MHz rate for machine-state execution. The on-chip features include two 16-bit timers, two 16-bit up/down counters, two PWM outputs, a free-running counter with two capture registers, two 4-bit real-time output ports, and an 8-bit A/D converter with four input channels. The devices come in 64-pin flat packs, quad-in-line packages, and plastic DIPs. In DIPs, the μPD78310CW, $15 (100); the μPD78312CS, $12 (5000).

NEC Electronics Inc, 401 Ellis St, Mountain View, CA 94039. Phone (415) 960-6000. TWX 910-379-6985.

Circle No 389



MICROPROCESSOR

The TMPZ84COOP-6 8-bit microprocessor operates at 6 MHz. The CMOS-processed μP is pin compatible with dual-in-line packaged NMOS Z80 devices, but uses only one-sixth the power consumed by the NMOS versions. The device has a standby current drain of 0.5 μA and an operating current of 15 mA. $3.30 (100).

Toshiba America Inc, 2692 Dow Ave, Tustin, CA 92680. Phone local office.

Circle No 390

SCSI INTERFACE

The single-chip 53C80 controller is functionally equivalent to the company's NMOS-based 5380 SCSI chip. The company has added four ground lines to minimize the harmful effects of ground-plane noise. The device features single-ended bus transceivers that enable the IC to drive the SCSI bus directly. It communicates with the μP as a peripheral device and is controlled by reading and writing several internal registers, which you can address as standard or memory-mapped I/O. The device supports bus arbitration and selection and reselection commands for prioritizing bus usage and performing concurrent I/O operations among different devices. Other hardware support includes parity generation and checking and the detection of a free bus or bus-phase changes. It supports DMA transfers of 1.5M bytes/sec. In a surface-mountable 44-pin plastic chip carrier or a 48-pin DIP package, $13.65 (1000). Delivery, eight weeks ARO.

NCR Corp, 1700 S Patterson Blvd, Dayton, Ohio 45479. Phone (513) 445-3467.

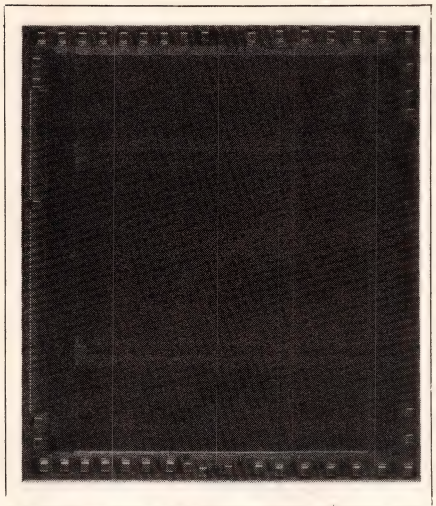
Circle No 391

16-BIT-SLICE μP

The Am29C101 is a cascadable 16-bit μP slice with a power consumption of 0.5W and a pin count of 64. (The company's earlier device was a 4W, 172-pin unit.) You can cascade multiple devices to achieve word widths of 32 bits or more. The device is microcode compatible with Am2901 designs. It has two independent addresses that access two data words simultaneously from the working register file. This 2-address architecture reduces the number of machine cycles and increases throughput. An 8-function ALU performs addition, two subtraction operations, and five logic functions on two operands; add and shift operations require only one cycle to perform. In a ceramic DIP package, $35 (100).

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 392

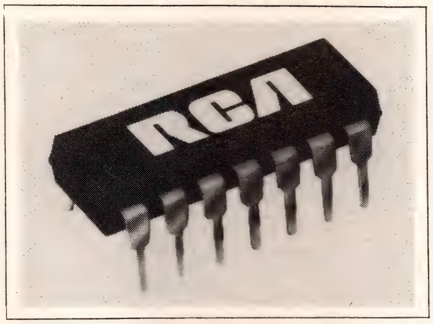


EPROM

The Am27C1024 is a 1M-bit device that features access time of 200 nsec and provides high-speed programming. The device is organized as 64k×16 bits. You can program 16 bits simultaneously in less than two minutes using the manufacturer's interactive algorithm. The 16-bit architecture allows direct interfacing with 16- and 32-bit systems. In standby mode, the device uses 5 mW; in power-down mode, it specs 1-mW power dissipation. In a 40-pin side-brazed package, $199 (100).

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 393



PARITY ICs

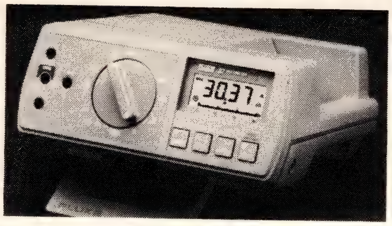
The CD54/74 HC/HCT280 9-bit parity generator/checker comes in an HC version for all-CMOS system designs and in an HCT version for direct interfacing with low-power Schottky TTL bipolar logic. The device accepts nine input bits. For either an odd- or even-parity result, typical propagation-delay time from I/O is 17 nsec at 25°C with a 5V supply voltage and 15-pF load. HC types operate over a supply-voltage range of 2 to 6V dc; HCT types operate over 4.5 to 5.5V dc. The devices operate over −40 to +85°C. The CD54HC/HCT280 comes in a 14-lead hermetically sealed ceramic DIP; the CD74HC/HCT280 comes in a 14-lead plastic DIP. $2.06 (100).

RCA Solid State, Rte 202, Somerville, NJ 08876. Phone (201) 685-7460.

INQUIRE DIRECT

CIRCLE NO 167

CIRCLE NO 197

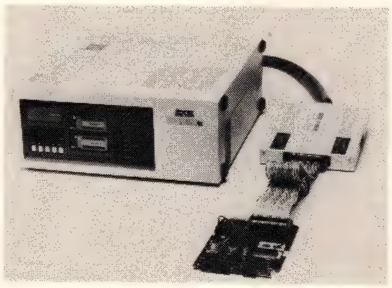


BENCHTOP DMM

The Model 37 3½-digit digital multimeter features a combined analog-digital display. The front panel has a 15° slope for visibility and switch access. A compartment built into the rear half of the case allows you to store test leads and small accessories inside the meter. The device features a 0.1% accuracy, a freeze-reading function, autoranging with manual range selection, and a continuity beeper. The unit operates from an internal 9V battery (1000-hour typ) or from line power with a battery eliminator. It meets UL 1244 requirements. All current ranges, including the 10A range, are protected by fuses. The resistance function is overload protected to 500V rms, and both ac and dc voltage functions are protected to 1000V rms. $229.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (206) 347-6100. TWX 910-445-2943.

Circle No 395



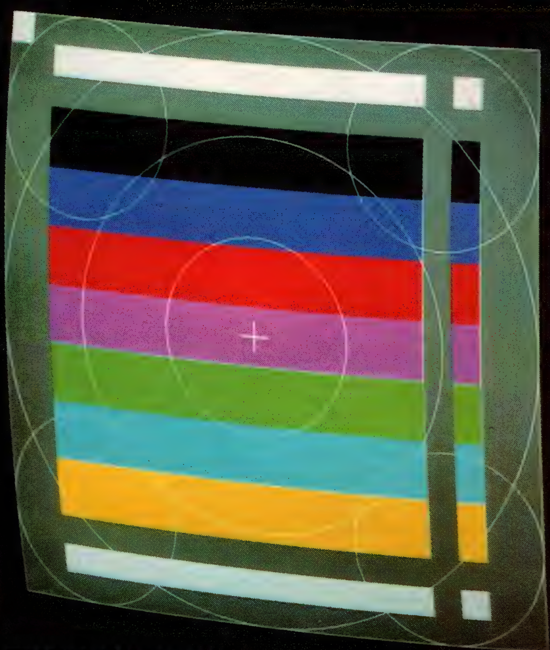
IN-CIRCUIT EMULATOR

The ICE-Engine/BX-8 universal real-time in-circuit emulator works with an IBM-PC or CP/M computer. It supports Z80, 8085, 6809, 8048, and Z80 CMOS series μPs (pods required). An 8051 pod is scheduled for mid-1986. The device includes a 64k-byte mappable emulation RAM, a 2k×40-bit trace memory, a 256-step register-trace memory, and a symbolic debugger. A resident debug-command language enables you to create a macroprogram that executes an emulation sequence automatically. Three hardware triggers control such functions as program break and real-time trace. Additional features include a built-in PROM programmer and eraser that supports 2716 to 27256 EPROMs; a battery-powered 32k-byte RAM file that retains data for as long as 30 days; and a hardware timer for measuring program-execution time. $3995. Additional pods, $990 ea.

Ziltek Corp, 1651 E Edinger Ave, Santa Ana, CA 92705. Phone (714) 541-2931.

Circle No 396

You Don't Need a Thousand Words When You Have a Picture Like This!



Unretouched photograph

**3.5 NS max. rise & fall time measured at CRT cathode.*

The image quality demonstrated here is required by your customers . . . and will be appreciated! They expect THE BEST from original equipment manufacturers. You can provide it! While other video monitor venders claim, "about 100 + MHZ" video bandwidth, **Video Monitors, Inc.** provides it! While other vendors claim, "full gray-scale color capability," **VMI** delivers it!*

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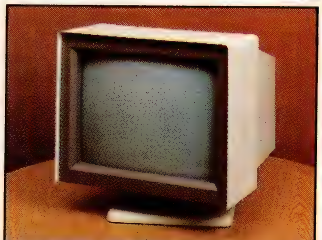
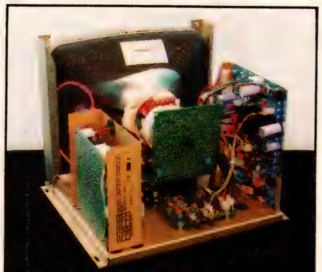
Large Image Area



Ergonomic Design



State-of-the-Art Technology

CIRCLE NO 168

Look at all the FACTs that go into computers.

When it comes to computer designs, there's one fact you shouldn't overlook: Fairchild Advanced CMOS Technology.

The highest performance CMOS logic family available, FACT is a comprehensive, rapidly growing product line. With a number of features ideal for computer applications from PCs to minicomputers.

Features such as higher speed. FACT's high-speed propagation delays are better than 5ns for gate functions and typically don't change more than 2ns over the entire operating voltage range.

Power consumption is just as impressive – typically 10 μW per gate quiescent, the lowest in the field. In fact, FACT uses 2-3 orders of magnitude *less* power than any competing technology. So your system reliability and packing densities are enhanced, power supplies can be made smaller, and heat dissipation hardware can be significantly reduced. In some cases, it's done away with altogether.

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There's still more:

FACT provides the highest noise immunity available. Its input protection diodes help suppress transient noise in your application. And FACT is available in SOICs, and plastic or ceramic DIPs.

For more information and a free FACT data book, call your local sales office or distributor. Or contact The Fairchild Customer Information Center at 1-800-554-4443.

Because it's time your computer designs took advantage of all the FACTs.

FACT™

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We're taking the high ground.

FAIRCHILD

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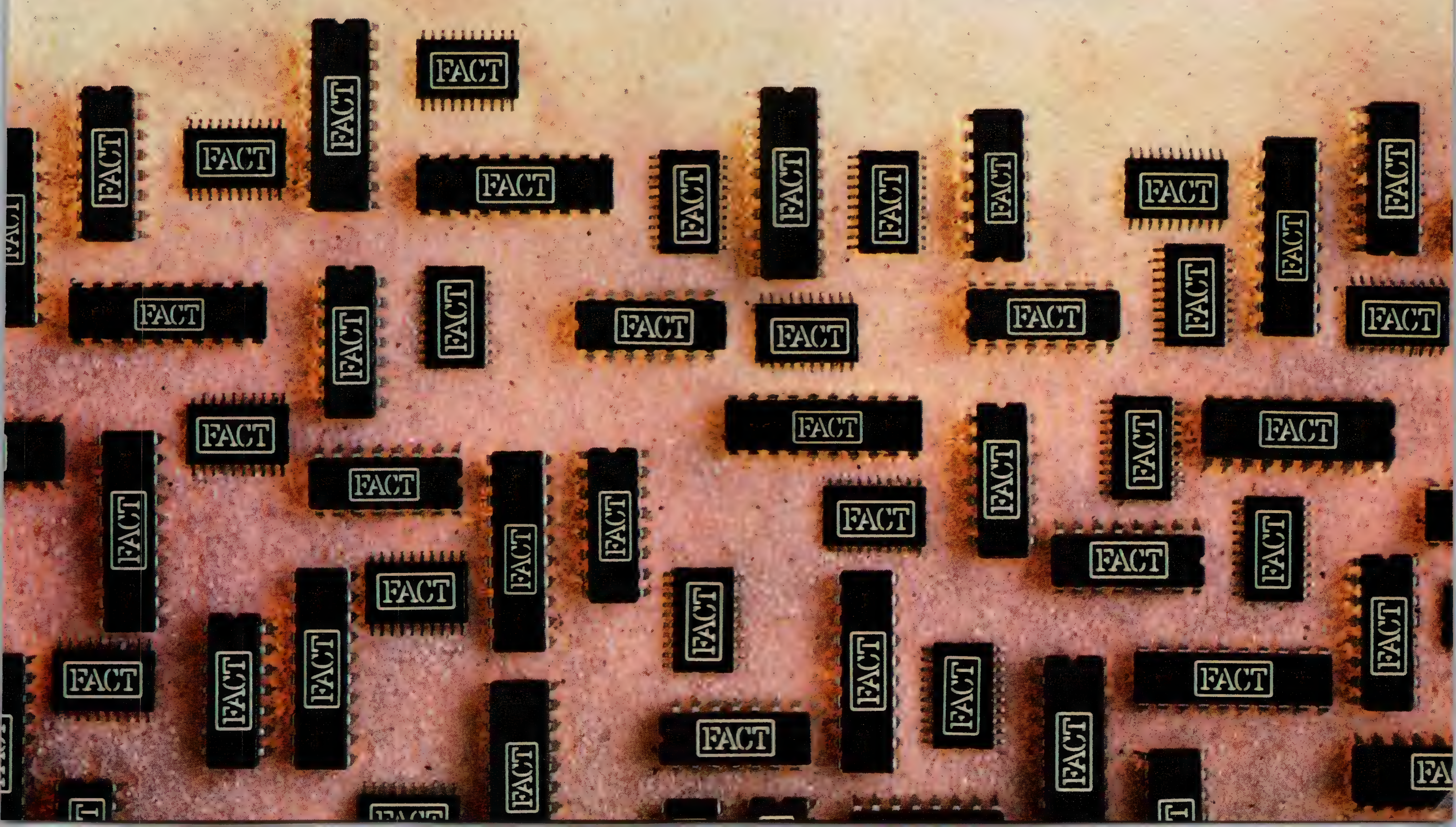
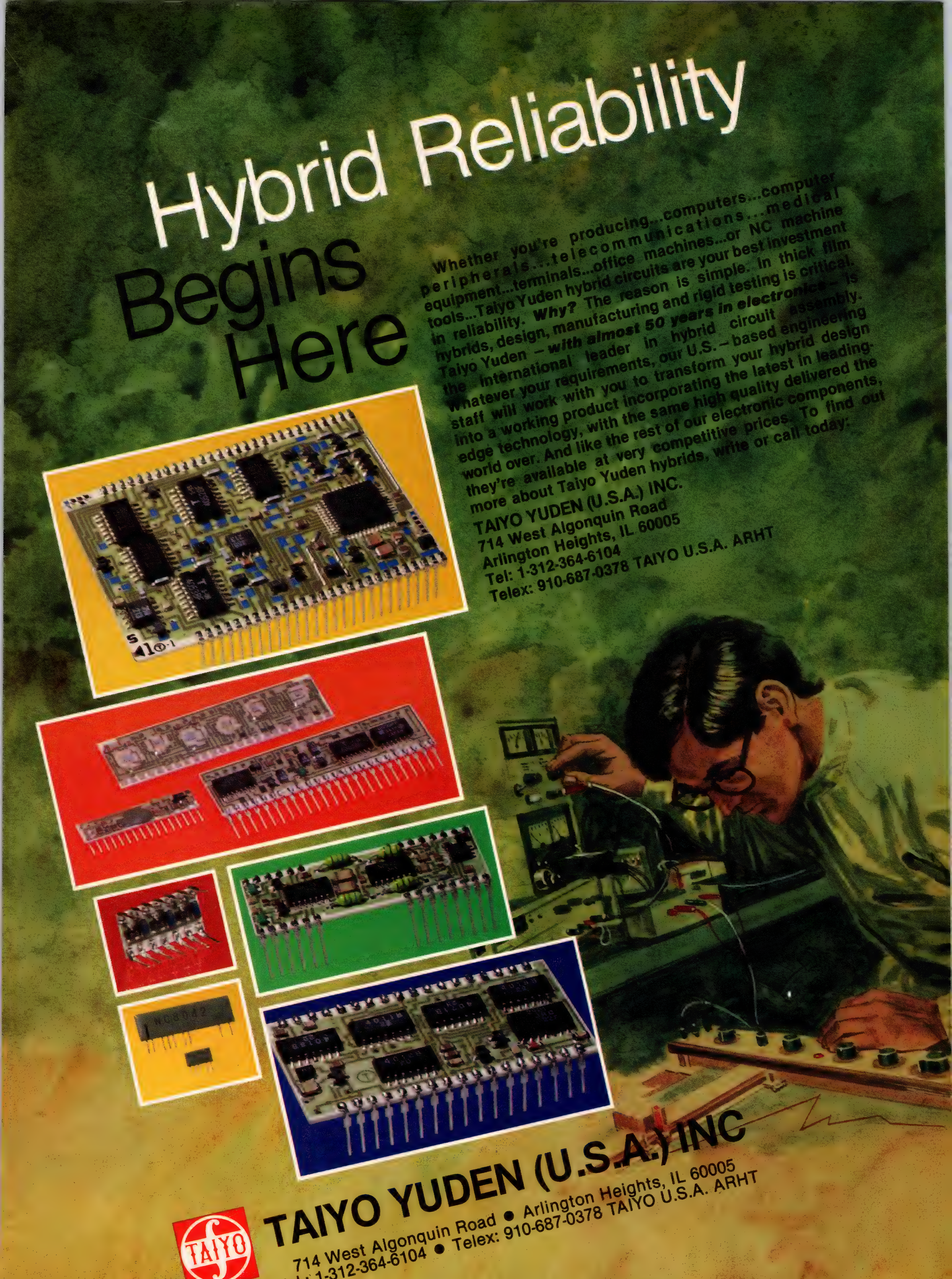
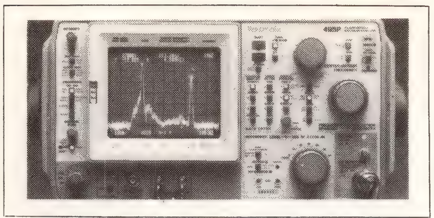




CIRCLE NO 170

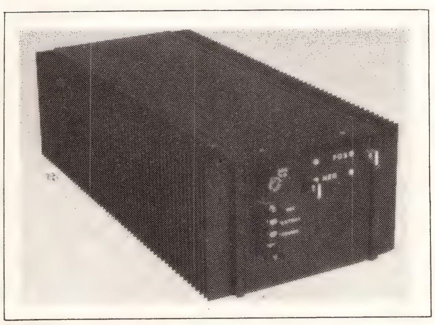


SPECTRUM ANALYZERS

The 495 and 495P spectrum analyzers cover frequencies ranging from 100 Hz to 1.8 GHz with −130-dBm sensitivity. Also included are a built-in frequency counter and signal processing for sorting continuous wave, pulsed RF, and other signals. An automatic bandwidth function marks and measures the occupied bandwidth, at a level you determine, after each sweep. With option 05 for macroprogramming, you can download frequently used measurement programs into nonvolatile memory of the instrument. This option also provides internal center- and dot-marker frequency accuracy to one part in 10^9. Switch-selectable 50 or 75Ω impedance is optional. A Help mode comes on the standard units; a MATE/CIIL language is optional. You can operate either analyzer to drive a plotter with no controller. The 495P is fully programmable and IEEE-488 compatible. 495P, from $28,950; 495, from $24,350.

Tektronix Inc, Box 500, Beaverton, OR 97005. Phone (800) 547-1512; in OR, (800) 452-1877.

Circle No 397



1500W SUPPLY

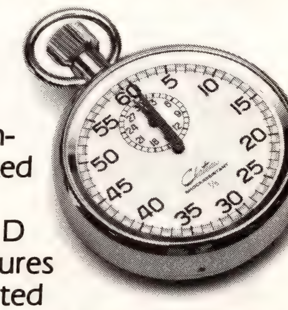
The Model 91008 convection-cooled, switching supply delivers 28V dc at 55A from a nominal 115V ac, 47- to 440-Hz single-phase source. The device operates over an ambient temperature range of 0 to 70°C. Cooling fans for air flow and cold plates are not required. Line and load regulation are ±1%. Noise and ripple is 300 mV p-p max. All units meet the environmental requirements of MIL-STD-810D for shock, humidity, vibration, salt, fog, and fungus. MTBF, calculated per MIL-HDBK-217D, exceeds 100,000 hrs. The device measures 8×5×17 in. and weighs <35 lbs. Other voltage and current combinations are available. $3500 (100). Delivery, 12 weeks ARO.

Power Ten Inc, 486 Mercury Dr, Sunnyvale, CA 94086. Phone (408) 738-5959.

Circle No 398

One Million Samples/Second

15-Bit Resolution



Preston Scientific's GMAD1A A to D Conversion Systems provide 1MHz conversion, 15-Bit resolution, and multiplexed inputs with up to 512 channels.
All of Preston's GM & EM Series A to D Conversion Systems include these features and more . . . such as software supported interfaces to DEC, Micro Vax, HP 1000, IBM PC and others.
Preston's building block concept results in a unique data acquisition sub-system that provides a wide variety of input channel signal conditioning and digital I/O options.

PRESTON

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805 East Cerritos Avenue
Anaheim, CA 92805
(714) 776-6400
TELEX: 510-100-4596

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For the ultra-wide bandwidth and low, flat insertion loss needed by broadcast or remote TV lines. For security, CCTV or Industrial Process Control systems. For high-speed Data Lines or Medical Imaging Equipment. Whatever your needs, there's a North Hills Isolation Transformer designed to meet them.
Engineered for unmatched reliability. Standard insulated BNC connectors for easy installation. Backed by a 3-year warranty—it's the widest selection of Wideband Isolation Transformers available anywhere. And it's available now! Right off the shelf!

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CIRCLE NO 172

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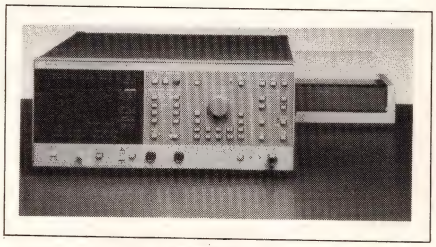
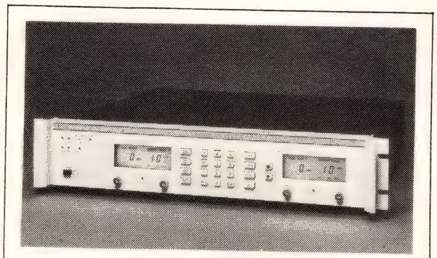


RF ANALYZERS

The 6400 line of RF analyzers includes the Model 6407 (1 to 1000 MHz), and the 6408 (10 to 2000 MHz). Each μP-controlled device is a combination signal source and scalar-network analyzer that makes transmission, return-loss, and absolute-power measurements from 1 to 2000 MHz with a dynamic range from 16 to 60 dBm. The analyzers offer drift-free performance. In addition to the integral CRT screen (7-in. diagonal), a large-screen display is available. Frequency accuracy is ±100 kHz; resolution is 10 kHz. Included are nine stored setups, eight markers, and four limit lines. The instrument weighs 35 lbs. $9430. Delivery, 16 wks ARO.

Wiltron Co, 490 Jarvis Dr, Morgan Hill, CA 95037. Phone (408) 778-2000. TLX 275227.

Circle No 399



2-CHANNEL FILTER

The Model 552 dual-channel programmable filter has full-scale sensitivity that is selectable in 5-dB steps from 1 mV rms (−60 dBV) to 10V rms (+20 dBV). You can program the cutoff frequency from 10 Hz to 50 kHz with 2-digit resolution. The fifth-order, elliptic filter with 0.5-dB ripple in the passband and >72-dB stopband attenuation yields a rolloff rate greater than 50-dB/octave. You can control the

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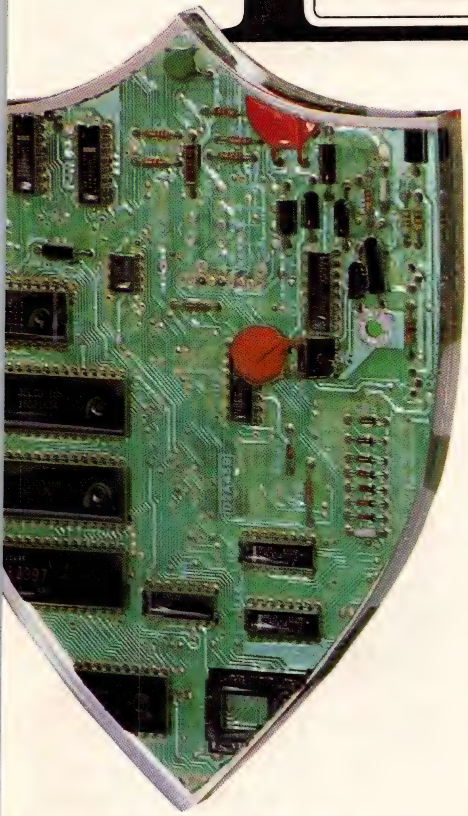
The Guide to Total Electronics Protection



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The protection of silicone, the processing ease of organics.

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Fast-cure coating for fiber optics.

OPTIGARD™ optical fiber coating UV-cures in just 0.3 seconds—5 to 20 times faster than thermal-curing coatings. And it protects against moisture and "microbends" better than acrylate coatings. It's part of the OPTIGARD family which includes fiber optics grade $SiCl_4$ core and cladding and OPTIGARD 5565 cable filler.

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In semiconductor-vacuum applications, pump fluids have to stand up to corrosive gases, heat and pressure. Dow Corning® 711 mechanical pump fluid meets the test and costs less than other inert fluids.

CIRCLE NO 86

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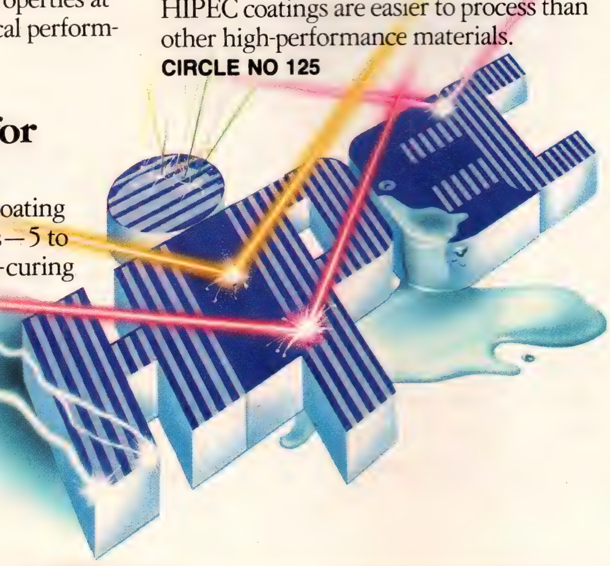
Stress. Moisture. Ion contamination. Voltage leakage. Alpha particles. All are killers of your devices, robbers of reliability. Now you have a defense against them. HIPEC® coatings protect semiconductors and hybrids through a wide range of temperatures and environments. They're available in a variety of forms from gel to firm elastomer and resins. And HIPEC coatings are easier to process than other high-performance materials.

CIRCLE NO 125



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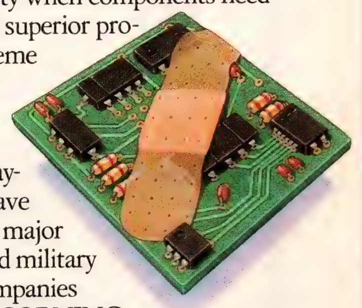
A PC board coating simply has to be reliable. And with DOW CORNING® 1-2577 conformal coating you get more: easy repairability when components need replacing. Add superior protection in extreme environments, versatile processing with dipping or spraying, and you have all the reasons major automotive and military electronics companies choose DOW CORNING 1-2577.



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There's more.

There's also our unique team of experts whose only mission is to develop and customize coatings, adhesives, dispersions, sealants, and components specifically for you. Supported by dedicated research and manufacturing facilities, we will help you meet tomorrow's challenges today. Ask about our Specialty Elastomers Group.

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Midland, MI 48686-0994.

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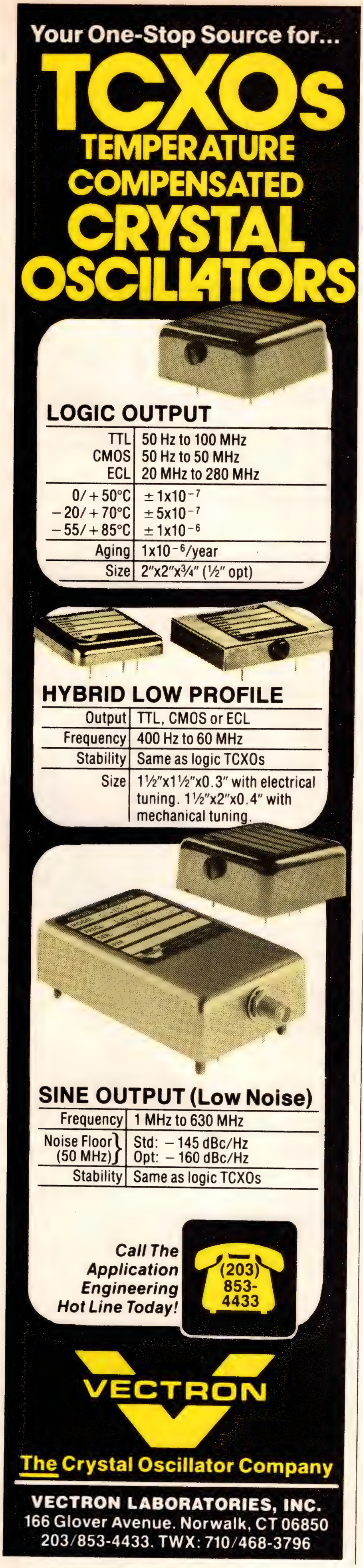


CIRCLE NO 173

device locally from the front-panel elastomeric keypad or remotely with either the IEEE-488 or RS-232C interface; the keypad and the two interfaces are standard. A digital display shows filter and gain parameters. $3500. Delivery, 10 to 12 wks ARO.

Wavetek San Diego Inc, Box 85265, San Diego, CA 92123. Phone (619) 279-2200.

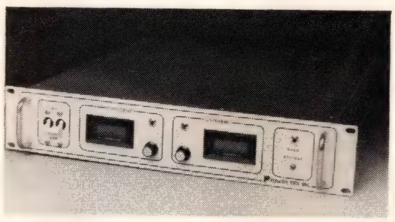
Circle No 400

SCOPE CRT CAMERA

The Primeline Model 7000 CRT camera works with oscilloscopes, test instrumentation, and computer terminals. You can hold the device when you use it with a large selection of hoods to fit display screens from 8×10 cm to 12 in. diagonally, or you can bezel mount it to most oscilloscopes. The camera uses standard black-and-white or color Polaroid film. It includes a variable-shutter control from 1/125 to 1 sec, a B option, and f-stops from f/3.5 to f/16. When mounted, you can swing it from side to side for an unobstructed view of the display, and you can remove it from the equipment when you're not using it. With hood included, $395.

Soltec Distribution, Box 818, Sun Valley, CA. Phone (818) 764-5400. TLX 4943094.

Circle No 401



2-kW SWITCHERS

The Series 3400 switching power supplies produce 2 kW in 3½-in.-high, standard rack-mountable packages and weigh 30 lbs or less each. These units are designed for system test or semiconductor and passive-component burn-in. They operate at 80 to 85% efficiency. Models are available with output ranges from 0 to 7.5V to 0 to 600V with output current levels as high as 250A. The supplies operate from a single-phase source of 95 to 127V or 190 to 253V ac, 47 to 63 Hz. Line or load regulation is 0.1%. Transient response is 10 msec on most models. The supplies operate at an ambient temperature of 0 to 50°C without derating. From $1050.

Power Ten Inc, 486 Mercury Dr, Sunnyvale, CA 94086. Phone (408) 738-5959.

Circle No 402

CALIBRATOR

The Versa-Cal calibrators have temperature sensors embedded within the binding post to maintain accurate reference-junction compensation even after severe changes in ambient temperature, according to the manufacturer. The calibrators feature 1-μV resolution and stability, 0.1° thermocouple-curve matching, and 0.005% full-scale calibration. Outputs range over −20 to +101 mV. Models are available with three or seven thermocouple ranges, plus a millivolt range as well as current-loop calibration capability. All standard thermocouple ranges, such as J, K, T, E, R, S, and C, are available as well as NM, B, D, G, N, PT2, and S-48. Four-range unit, $1445; 8-range unit, $1495. Delivery, six weeks ARO.

Biddle Instruments, 510 Township Line Rd, Blue Bell, PA 19422. Phone (215) 646-9200. TLX 834423.

Circle No 403

L02
Second in a series on the performance and flexibility of ZAX emulators.

Communication, coordination and cooperation in action. It's the same at ZAX.

"If you think power, speed and sophistication are all you need in an emulator, take a lesson from a Formula One team"

The Formula That Determines Number One

The World Driving Championship is contested in vehicles which represent the absolute pinnacle of power, speed and sophistication in motor racing: Formula One.

Their engines are smaller than a VW bug's, yet they produce a formidable 1000+ horsepower. Speed? Formula One cars can blister the pavement from 0 to 100 mph before you can finish reading this sentence. The sophistication level is astonishing: Disk brakes made from carbon fiber-reinforced plastic, 7-speed transmissions, intake and exhaust valves that actuate from compressed air rather than conventional springs.

Yet, behind all the impressive numbers and sleek shapes, there remains a less flamboyant activity that no driver could complete a lap without–*communication.*

We think it's the same with our emulators.

Communication: The Key to a #1 Development System

At ZAX, we too build power, speed and sophistication into each of our ICD-series emulators. And something more—proficient communication. Because emulators that can communicate ensure you of a more flexible operating environment and additional emulation features.

ZAX emulators can be controlled by any terminal utilizing RS-232 interface. This allows you to use a full-size ASCII keyboard and large CRT for easy viewing and control. So now you can see the output of your input. And RS-232 interface means unrestricted use of personal and mainframe computers via ZAX's ZICE communications utility. (You can also control our emulators with a terminal or PC and then download code from a mainframe for workstation efficiency.)

The Logic of a Logic-State Analyzer Interface

Our newest communication feature allows each of our emulators to directly interface with any standard logic-state analyzer connector. This potent combination merges an LSA's sophisticated trigger, qualification, data-acquisition and measurement capabilities with our emulator's debugging mechanisms and memory facilities.

Choose from an extensive line of manufacturer's software products, and the complete package results in a modular development system that's powerful, fast, sophisticated and communicates with *your* current equipment inventory—economically.

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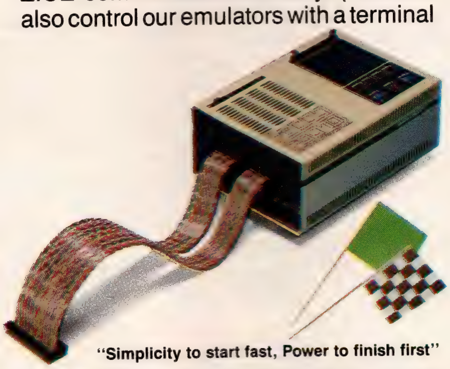
For information on other ZAX emulator features and news about entire product line, call us **toll free 1-800-421-0982** (714 474-1170 in California). Or write us at ZAX Corporation, 2572 White Road, Irvine, CA 92714. Telex 183829.



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ZAX In-circuit emulators for Z80, 6809/E, 68000 family, 8048 family, 8051 family, 8085, 8086/88 & 80186/88, and V20/V30 processors.

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The INMOS IMSG170 Color Look-up Table offers a grown-up solution to video display color enhancements. It lets you and your RGB analog display advance to a palette of more than a quarter million colors.

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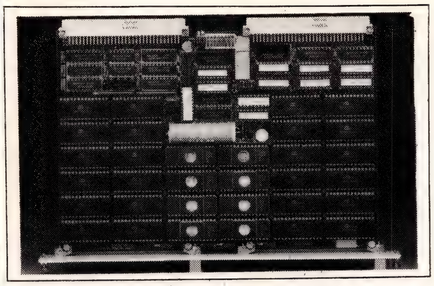


MEMORY CARD

Providing 32 byte-wide memory sockets, the CC-86 double Eurocard VME Bus memory board allows you to install as much as 2M bytes of EPROM. The sockets also accept static RAM devices. The memory map is divided into four blocks, which you can configure to different sizes according to the board's static-RAM and EPROM mix. Onboard battery backup and power-monitoring circuitry protects RAM data during power failures. The module supports byte, word, long-word, and unaligned VME Bus data transfers, and has a selectable address range, a base address, and address modifier decoding. The board has an operating range of 0 to 70°C and typically draws 1A from the 5V supply with no memory devices installed. From $800 to $1900, depending on population.

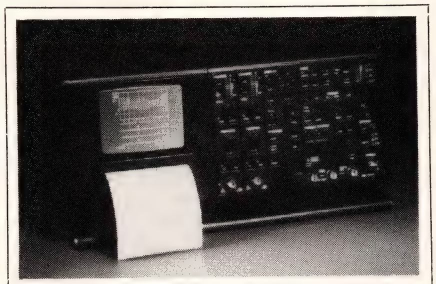
Compcontrol bv, Stratumsedijk 31, 5611 NB Eindhoven, The Netherlands. Phone (040) 124955. TLX 51603.

Circle No 404

Compcontrol Inc, 15466 Los Gatos Blvd, Suite 109-365, Los Gatos, CA 95030. Phone (408) 356-3817. TWX 510-601-2895.

Circle No 405

DIGITAL SCOPE



The SE571 2-channel digital-storage oscilloscope features an integral thermal printer that provides a hard copy of captured waveforms. You can also use it as an 8-channel, 25-MHz logic analyzer. The storage scope samples each of its analog input channels to 8-bit resolution at 25 MHz, allowing you to reconstruct input waveforms with frequencies as high as 10 MHz by nonlinear SI-interpolation. An aliasing warning indicator activates if the selected sampling rate is too low for faithful reconstruction of the signal. In logic-analysis mode, you can set up a binary trigger word and produce data either as a timing diagram or as an alphanumeric list. A combinational mode allows you to capture one analog signal and four logic signals simultaneously. The oscilloscope incorporates autozero

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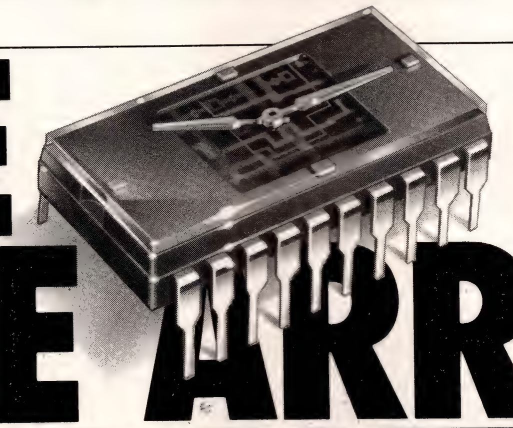

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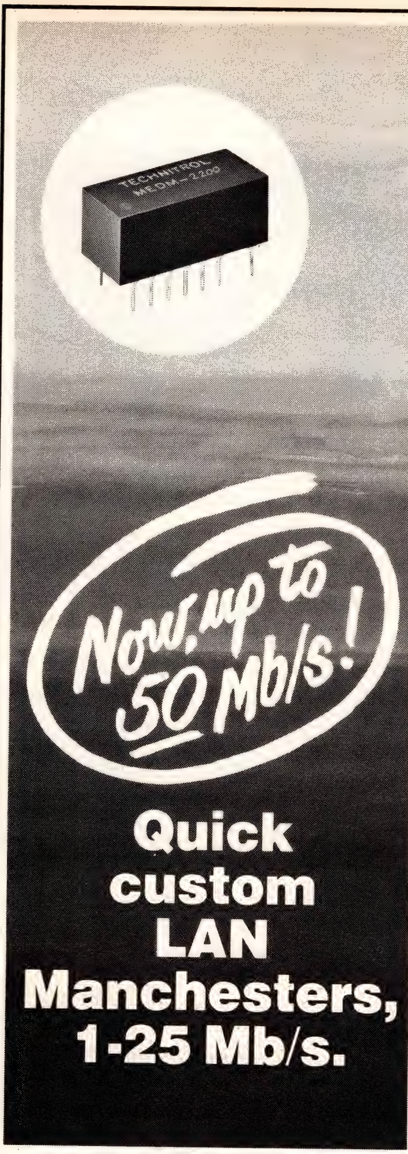

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circuitry to eliminate zero drift, and automatic input-range selection. Twin cursors allow you to evaluate captured traces for voltage, time, and frequency measurement. Additional features include nonvolatile storage of as many as eight instrument setups and waveforms, a real-time clock, and an optional IEEE-488 interface. $6500.

BBC-Metrawatt/Goerz, Thomas-Mann-Strasse 16-20, 8500 Nuremburg 50, West Germany. Phone (0911) 8602345. TLX 623729.

Circle No 406

BBC-Metrawatt/Goerz, 2150 W 6th Ave, Broomfield, CO 80020. Phone (303) 469-5231.

Circle No 407

PROTECTION DIODES

These transient-overvoltage-protection diodes, the Powerzorb Series, are available in two versions, with 1-msec exponential pulse-power ratings of 1.5 or 5 kW. The line covers the voltage range from 5.6 to 400V and exhibits a foldback characteristic after avalanche breakdown has occurred. The turn-on characteristics of the protection diodes allow you to use them to clamp the secondary effects of electromagnetic pulse radiation. The 1.5-kW units are available in standard DO-27A or DO-13 packages; the 5-kW devices are encapsulated in nonstandard packages. £0.50 to £0.60 for 1.5-kW devices; £1.00 to £1.20 for 5-kW devices (10,000).

Semitron Ltd, Cricklade, Swindon, Wilts SN6 6HQ, UK. Phone (0793) 751151. TLX 44848.

Circle No 408

SWITCHING TRANSISTOR

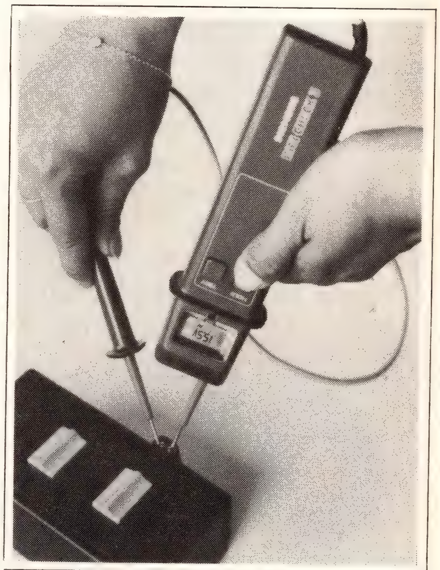
The SGSD00035 Fastswitch transistor has a safe-operating-area characteristic that eliminates the need for crossover-protection circuitry in many applications. Rated at 1000V and 12A, it operates at switching frequencies as high as 70 kHz. Used in forward-converter switch-mode power supplies, the transistor is suitable for power outputs between 250 and 350W and allows you to design compact supplies with low heat-sinking requirements. The transistor is available in TO-3, TO-220, and SOT-93 packages. Approximately $2 (1000).

SGS-Ates, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (39) 65551. TLX 330131.

Circle No 409

SGS-Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100.

Circle No 410



VOLTAGE TESTER

The D422 handheld tester measures dc and ac voltages as high as 999V and displays measured values on an LCD. A display indicator alerts you to voltages greater than 1 kV. The autoranging unit achieves a resolution of 0.1V for inputs to 60V. You can also use the tester to perform polarity-conscious continuity tests and semiconductor junction checks with the aid of an audible tone indicator. The battery-powered tester includes a low-battery indicator and is approved for DIN VDE-0680 Part 5 standards. DM 140.

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

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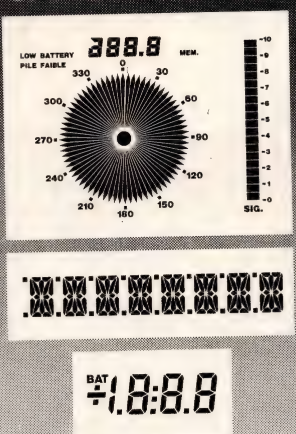

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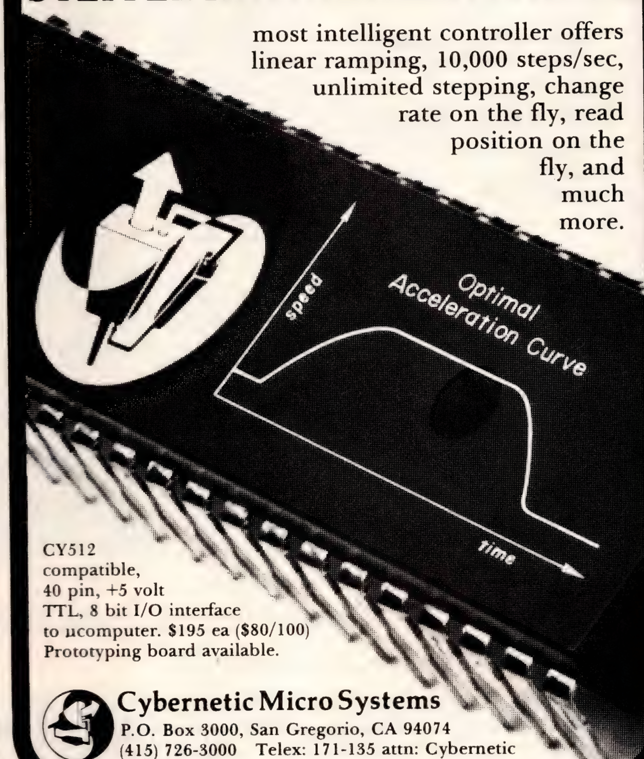

CY512 compatible, 40 pin, +5 volt TTL, 8 bit I/O interface to μcomputer. $195 ea ($80/100) Prototyping board available.

Cybernetic Micro Systems
P.O. Box 3000, San Gregorio, CA 94074
(415) 726-3000 Telex: 171-135 attn: Cybernetic

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The output-current capability of the LS1240A 2-tone telephone-ringer chip is sufficient to drive low-cost dynamic transducers with impedances as low as 300Ω. You externally program both the tone frequency and the alternation rate between the two tones. An internal polarity-guard bridge and a protection zener allow you to connect the device directly to the telephone line, and the IC's low current consumption allows you to operate four devices in parallel on one line. Supplied in a plastic miniature DIP, the LS1240A is pin compatible with standard LS1240 devices. Another version, the LS3240, has a bridge output and can drive high-impedance piezoceramic tranducers or an audio transducer and a visual indicator in unison. The LS1240A, approximately $0.50 (10,000).

SGS-Ates, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (39) 65551. TLX 330131.

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SGS-Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100.

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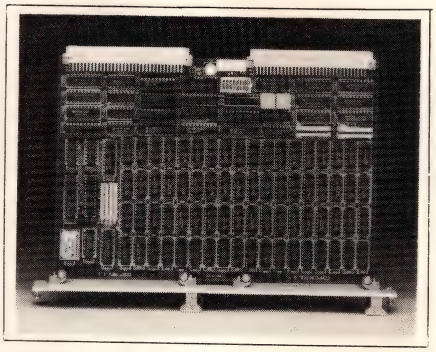

MEMORY BOARD

The CC-87 double Eurocard VME Bus memory board provides you with 2M bytes of dynamic RAM. It supports byte, word, long-word, and unaligned VME Bus data transfers, allowing you to use it with 8-, 16-, or 32-bit data-bus masters. Byte parity-checking logic is also provided. You can set the base address of the RAM on any 2M-byte boundary within the full 4G bytes of VME Bus address space, and you can program the address modifier decoding. The RAM has a typical read-access time of 290 nsec, a typical write-access time of 200 nsec, and a minimum cycle time of 320 nsec. The board typically consumes 1.6A from the 5V supply and operates over 0 to 70°C. $1295.

Compcontrol bv, Stratumsedijk 31, 5611 NB Eindhoven, The Netherlands. Phone (040) 124955. TLX 51603.

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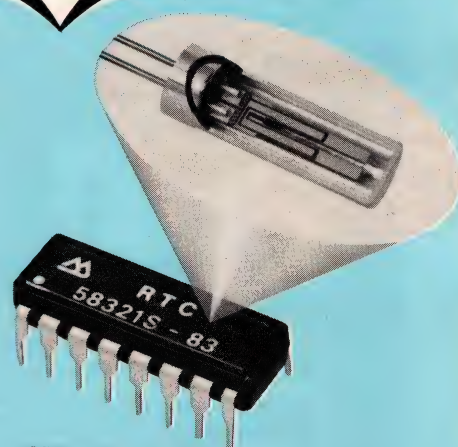

SPECIFICATIONS:
Realtime Clock Module RTC-58321

Quartz Frequency:	32.768 KHz
Precisions:	±10 ppm, ±50 ppm
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Introduced only recently, this powerful new series of logic analyzers is already successfully overcoming the traditional dominance of Tektronix by offering easy to learn, easy to use features the giant either doesn't have—or can't offer at a competitive price.

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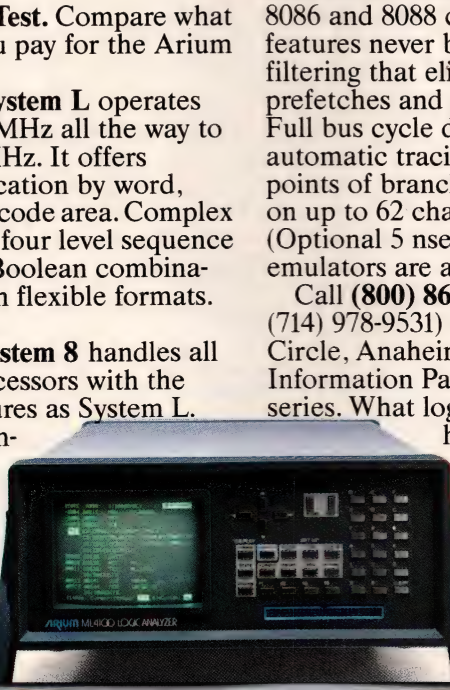
For just $4,685, System 8 handles all major 8-bit microprocessors with the same speed and features as System L. Then it adds disassembly, including all exceptions and bus cycles, built-in non-volatile memory, automatic test sequencing, powerful search and compare, eight saved set-ups, and RS-232C communications. Its price: $4,685.

For merely $5,850, System 16 gives you all the features of System 8, then adds troubleshooting of 68000, 68010, 8086 and 8088 chips with powerful features never before available. Prefetch filtering that eliminates unexecuted prefetches and prevents false triggering. Full bus cycle display. Jump mode™ for automatic tracing of start and stop points of branches. Cycle unscrambling on up to 62 channels. And all for $5,850. (Optional 5 nsec glitch pod and ROM emulators are also available.)

Call **(800) 862-7486** (in California (714) 978-9531) or write 1931 Wright Circle, Anaheim, CA 92806, for free Information Pack on the Arium 4100C series. What logic analyzers should have been from the beginning.



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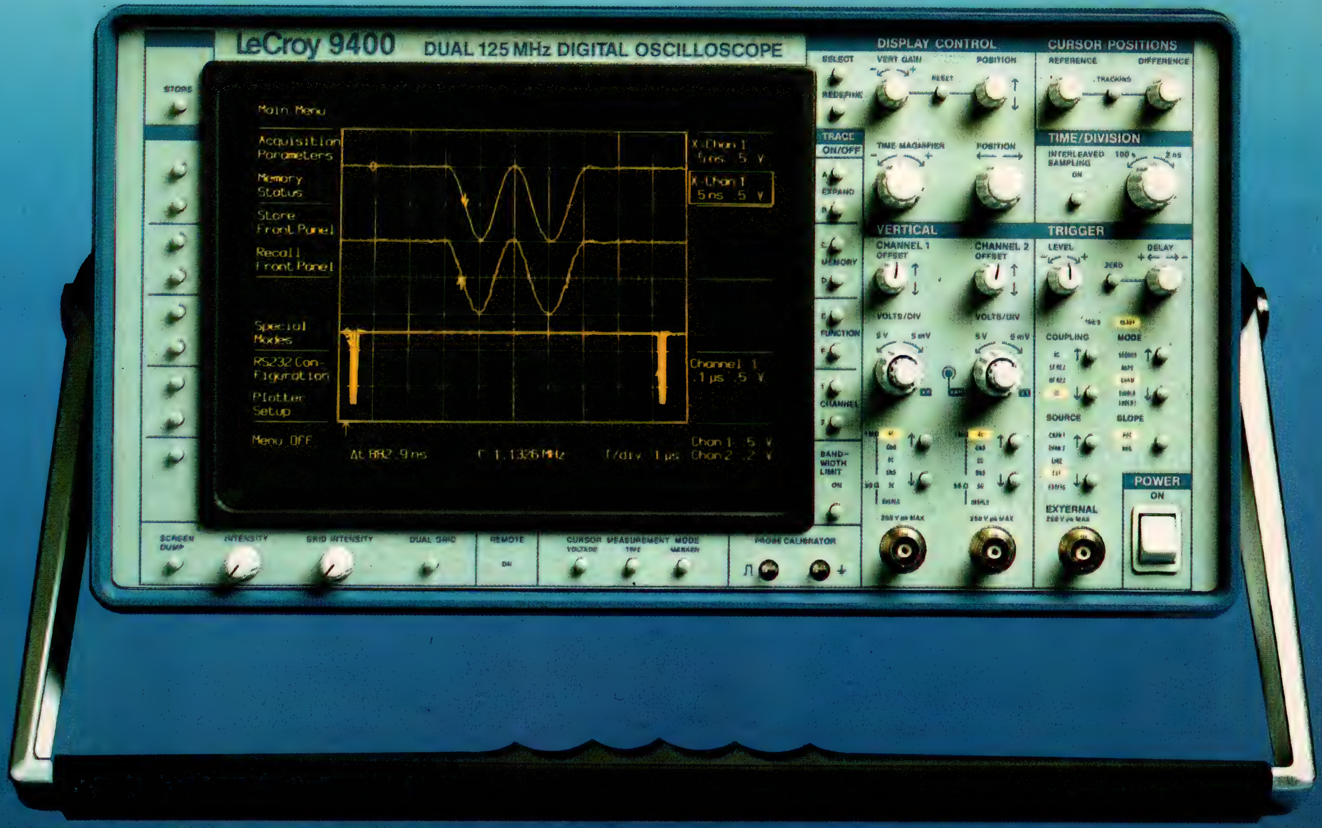

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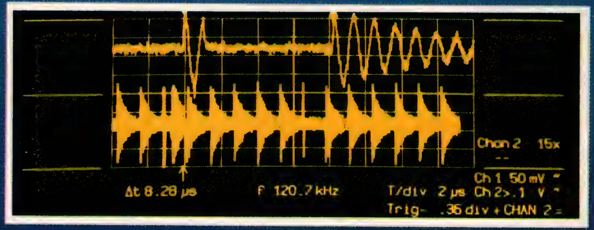
ACCURACY. Time measurements can be done with *0.002% accuracy*. The vertical accuracy of a standard 9400 is *± 2%* or optionally even *± 1%*. This means the 9400 is as much as *3 times* more accurate than any other scope today.

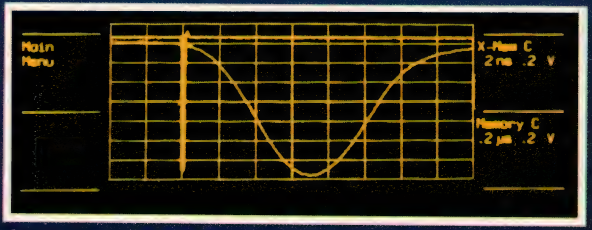
For detailed inspection of your acquired waveform, the 9400 features the exclusive *Dual Zoom* mode for up to 100 times expansion. Dual Zoom gives you two expanded traces per signal source - and when you increase the x-factor, precision and resolution improve, not deteriorate as in DSOs with shorter record lengths.

DISPLAY. The extra-high-resolution large display does full justice to the 9400's exceptional precision. *Vector graphics*, unlike raster scans, show continuous traces, finely detailed, razor sharp, without jaggies. The 1,000 × 1000 point resolution even exceeds that of a normal analog scope.

★And there is much more to say about this versatile and cost effective ($ 9900 base*) DSO. **Call us now...for details and a demonstration!!**

*USA price list only.





Top: Dual zoom and time cursors are applied to measure delay between double pulses with 100 ps resolution and 0.002% precision.

Middle: Channel 2 is segmented in 15 partitions of 2,000 words each. Expansion of event #3 appears on top.

Below: A 10 ns wide pulse is digitized with 5 Gs/s interleaved sampling speed. Expansion to 2 ns/div shows outstanding time and screen resolution.

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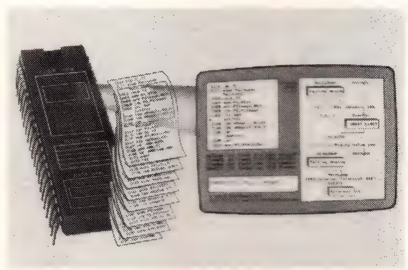
ALP Systems, 190 W 800 North, Provo, UT 84604. Phone (801) 375-0090. TLX 453195.

Circle No 416



SIMULATOR/DEBUGGER

The Sim8096 debugger allows designers to debug 8096 code on IBM PC/XT and PC/AT workstations. The multiwindow display shows the source code, registers, stack, memory locations, timers, I/O ports, and pins. It also documents the program flow. You can either scroll through the source code without executing it, single-step through the code, or run full speed until a breakpoint is hit. You can also set register traps. Sim8096 allows you to embed I/O stimulus commands in the source code itself to exercise various I/O routines during stepping. You can issue I/O commands from the keyboard at any time for total flexibility. You can access the internal structures such as the A/D converter, the CAM and FIFO, the UART, various timers, and the interrupt structure. After debugging a program, you can dump the flowgraph and trace code to the system printer, thereby providing clear documentation for the code. The company also offers an 8096 cross-assembler for the IBM PC and an EPROM programmer that uses the

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CIRCLE NO 183

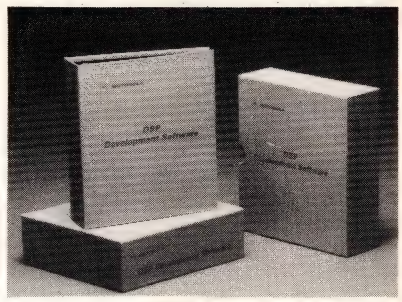
IBM RS-232C channel. The same HEX file that is used for debugging can be put into an EPROM. Sim8096 debug/simulator, $995; Cys8096 cross assembler, $295; EPROM programmer, $245.

Cybernetic Micro Systems, Box 3000, San Gregorio, CA 94074. Phone (415) 726-3000. TLX 171135.

Circle No 417

SIMULATOR/ASSEMBLER

The DSP56000SASMA simulator and assembler is a software package for the company's DSP56000 general-purpose digital signal processor, which will be available early in 1987. The company supplies two diskettes, one containing the simulator program, and the other containing the macro crossassembler program.



This package will allow you to begin incorporating the DSP as part of your system plans well before the actual part is available. The simulator program simulates the operation of the DSP on a clock-cycle-for-clock-cycle basis and yields measurements of actual code execution times. All on-chip pertinent peripheral operations, memory, and register updates are also simulated. The simulator executes DSP object code generated from either the macroassembler program or the single-line assembler in the simulator. You can define breakpoints and implement the single-step mode to view the execution of individual instructions. You can also set the program to run for a specified number of instructions or cycles. Built-in functions include transcendental math computations; arbitrary expression evaluation with bit shifting, Boolean expressions, and modulo operations; directives to define fixed-size modulo and reverse-carry data buffers; and separate load- and run-time location counters to facilitate the use of program overlays. $295.

Motorola Inc, Microprocessor Products Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone local office.

Circle No 418

TERMINAL EMULATOR

AST-5250/Async Dial-up enables a remote IBM PC, PC/XT, PC/AT, or compatible to communicate asynchronously with an IBM minicomputer by emulating the 5251/11 display terminal. This software works with the company's AST-5251/11 boards, which connect a local IBM

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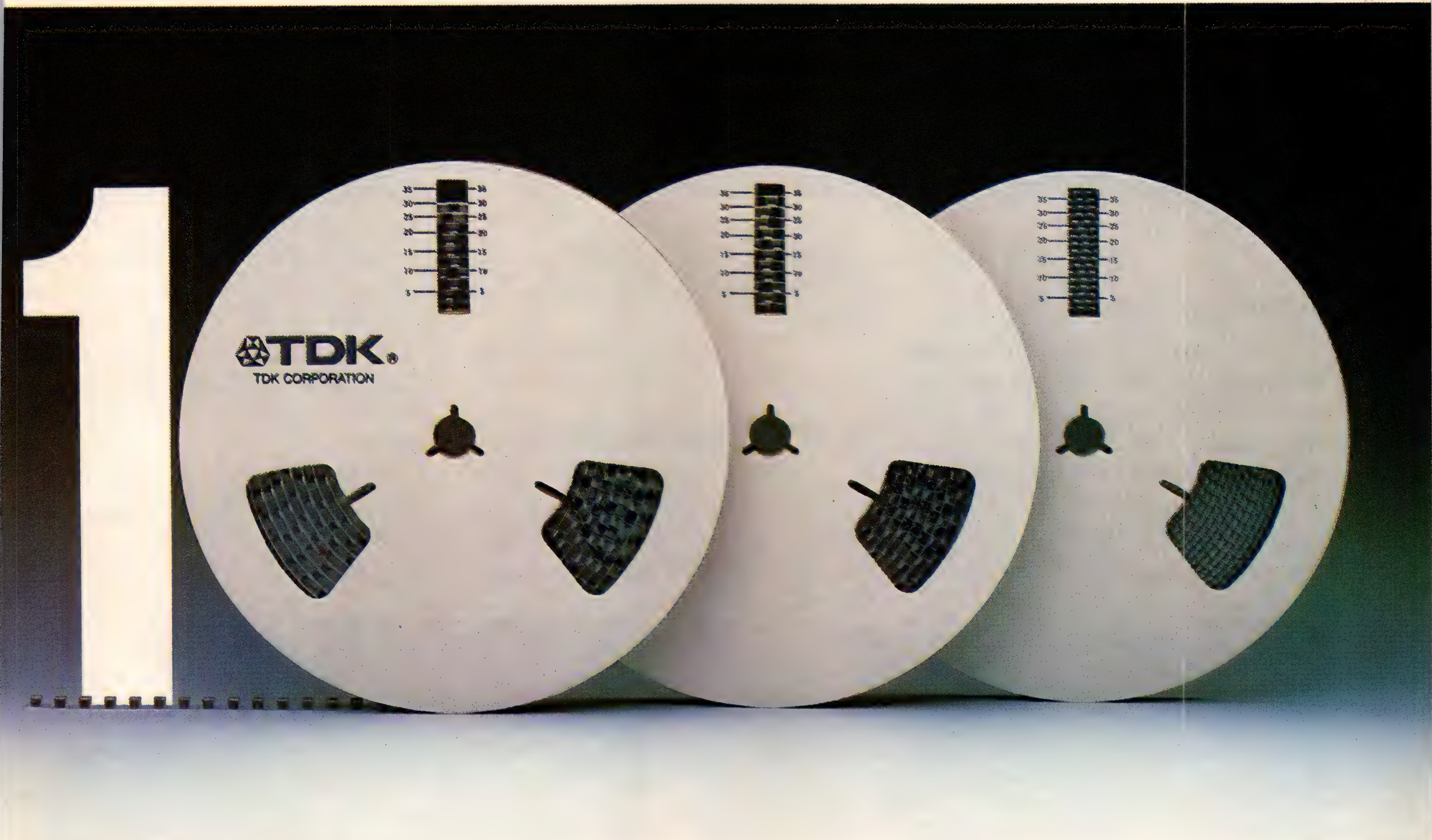

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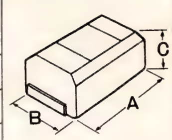
NL 3.2 x 2.5 x 2.2	0.12~220	30~60
NL 4.5 x 3.2 x 3.2	1.0~1,000	40~70
NLF 4.5 x 3.2 x 3.2 (shielded)	1.0~1,000	50~80



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The ASM180 crossassembler package provides program-development facilities for the Hitachi HD64180 µP. The package includes the relocatable macroassembler and linking loader, with an optional object module librarian. Features of the assembler include nested macros, conditional assembly, symbolic addressing, relative addressing, and generation of a symbol cross-reference listing. The INT180 is a symbolic debugger that simulates all aspects of the 64180 including interrupts, timers, serial I/O, 256 bytes of I/O space, and as much as 512k bytes of memory address space. This symbolic debugger/simulator can operate in both interactive and batch modes. Both the assembler and simulator/debugger are available on the DEC VAX/VMS, VAX/ULTRIX, and MicroVAX/VMS. ASM180, $2000; with object-module library, $2300; INT180, $1500.

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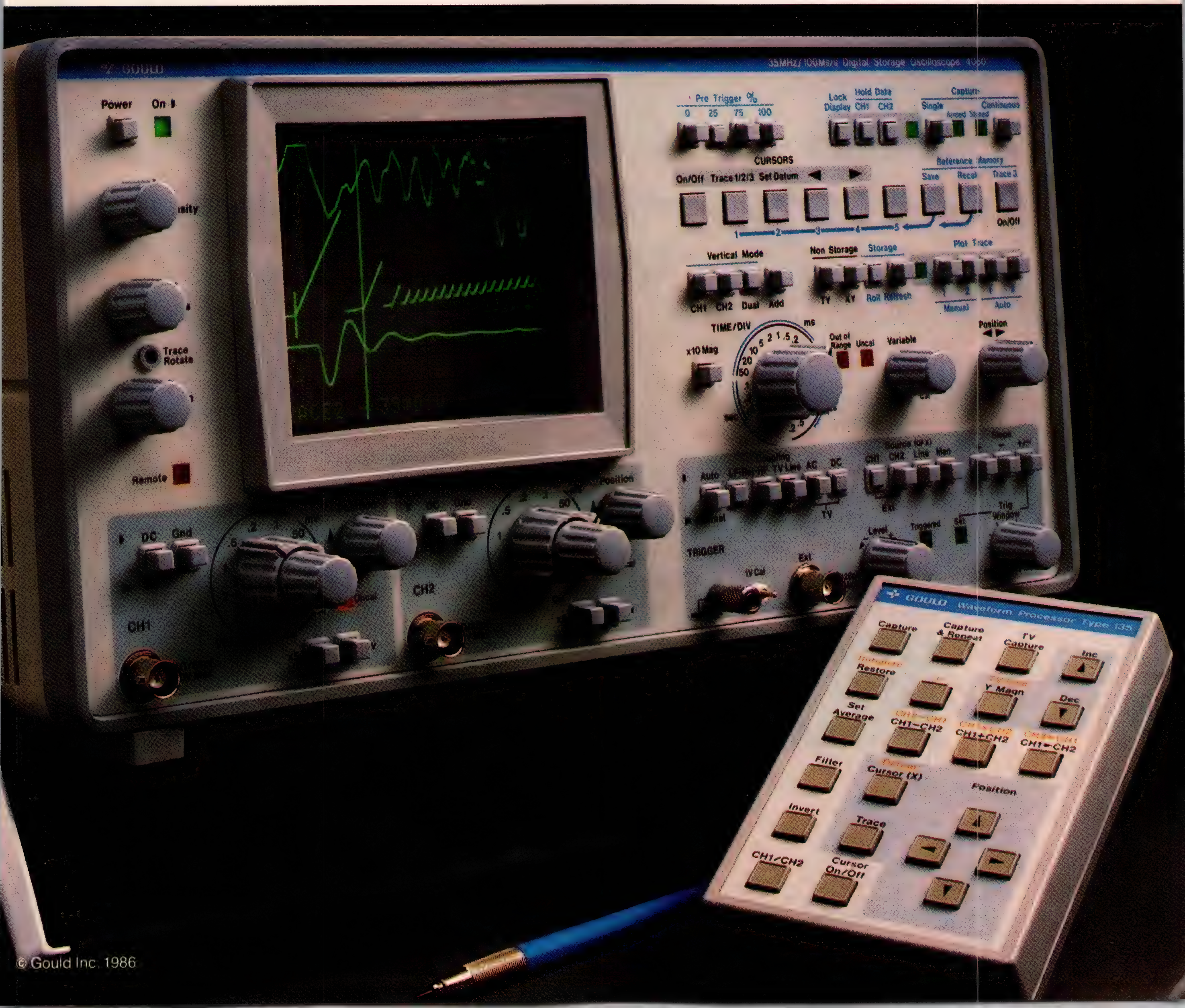

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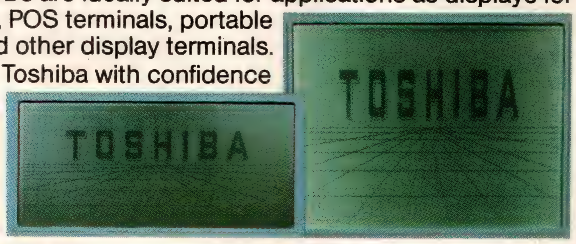

TLC-363 *TLC-402*

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W×H×D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° ~ 70° C	−20° ~ 70° C
Operating Temperature		0° ~ 50° C	0° ~ 50° C
Supply Voltage	VDD	7 V	7 V
	VDD − VEE	20 V	20 V
Input Voltage		0≤VIN≤VDD	VSS≤VIN≤VDD
Recommended Operating Conditions			
Supply Voltage	VDD	5±0.25V	5±0.25V
	VEE	−11±3V Var.	−11±3V Var.
Input Voltage	High	VDD − 0.5V min.	VDD − 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 − 35 degrees	15 − 35 degrees

Design and specifications are subject to change without notice.

TOSHIBA

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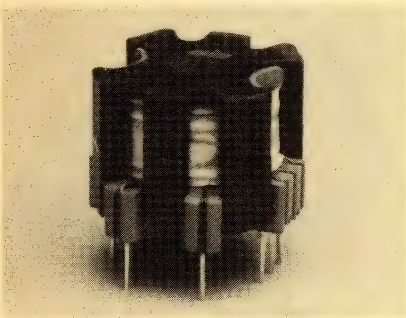

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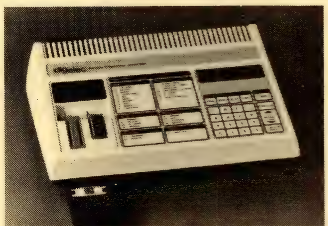

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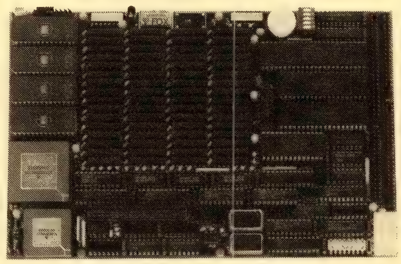

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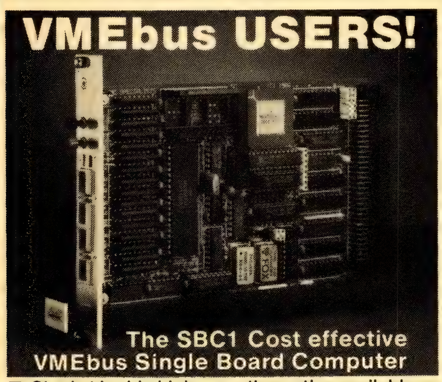

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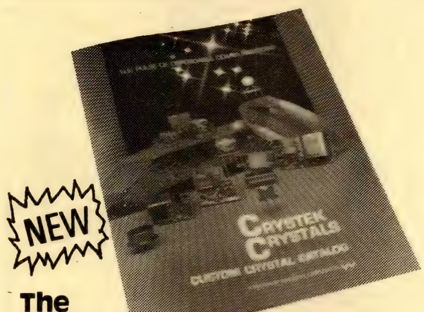

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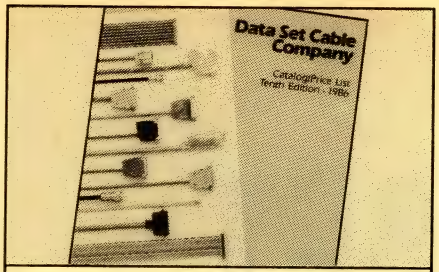

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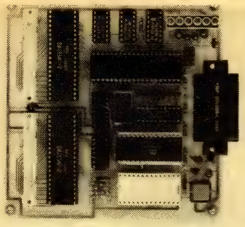

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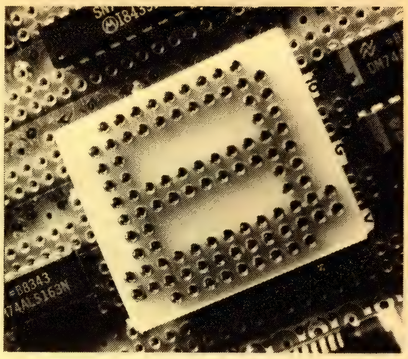

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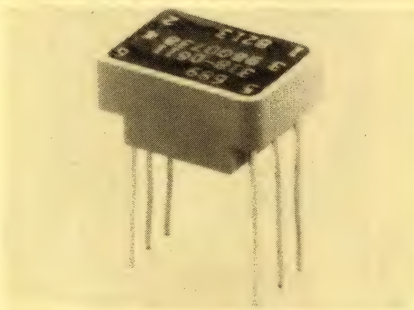

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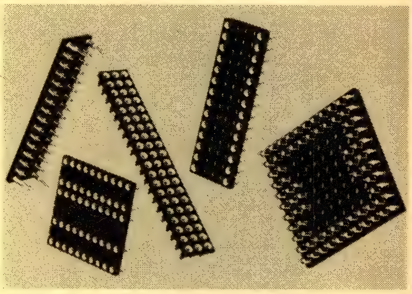

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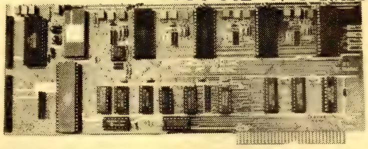

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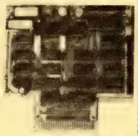

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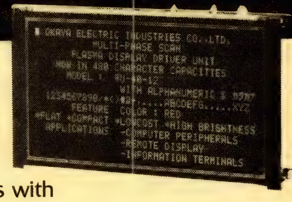

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68020

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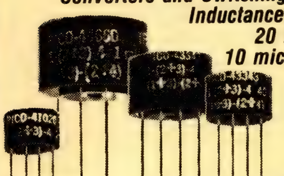

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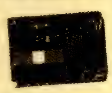

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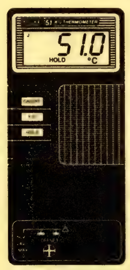

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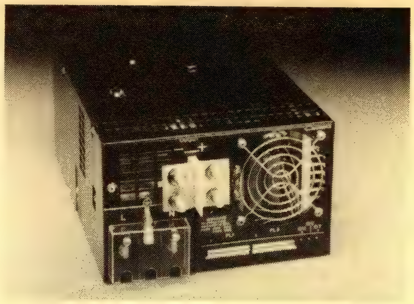

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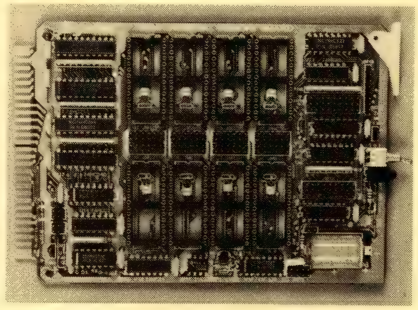

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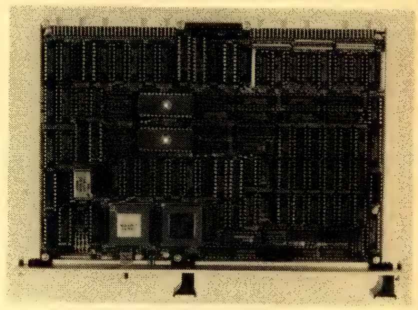

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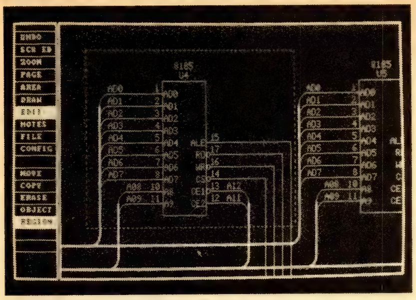

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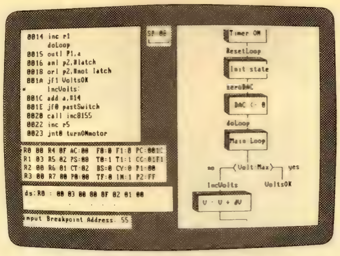

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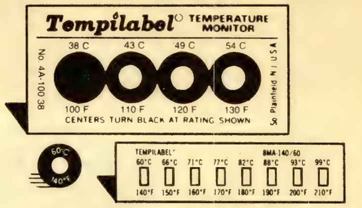

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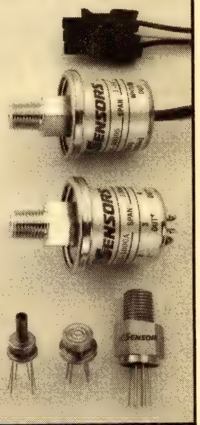

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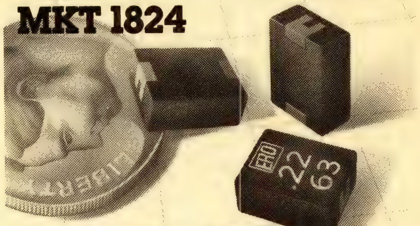

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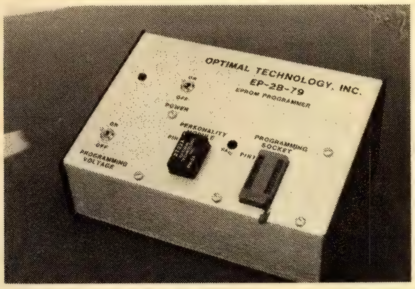

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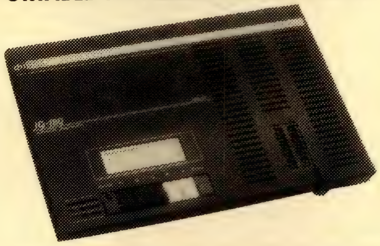

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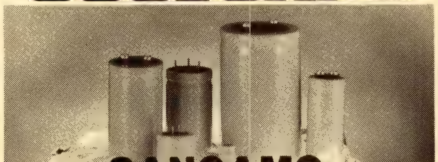

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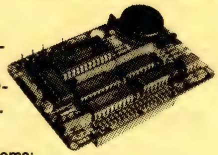

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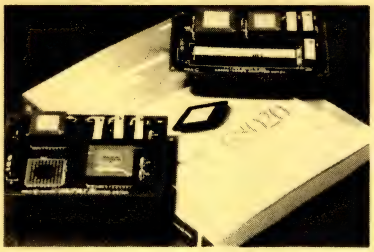
68020
Big Performance Boost!



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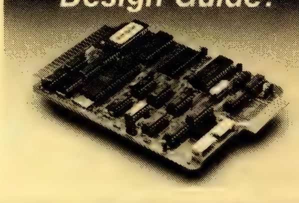

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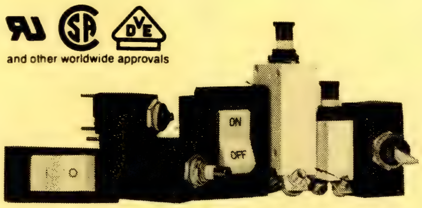

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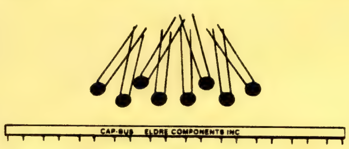

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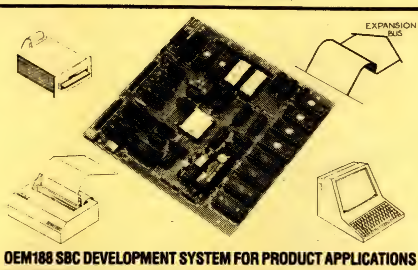

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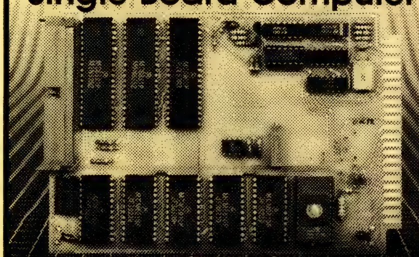

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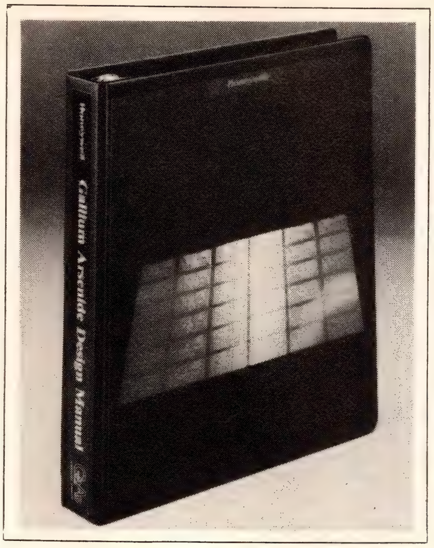
Brochure aids in choosing PLDs

This brochure describes the manufacturer's line of programmable logic devices available for volume production design (PALs, ProPALs, HALs, and ZHALs) and helps you decide which type you need. The pamphlet includes specification guidelines, a sample flow chart, a graph, and a checklist. The brochure also contains a table that lists the character and line limitations for the most common packages.

Monolithic Memories Inc, 2175 Mission College Blvd, Santa Clara, CA 95050.

Circle No 422

Manual provides design rules for ICs



The *Gallium Arsenide Design Manual* contains enough information to enable an IC designer to use the company's GaAs production technology—a 1-μm, depletion-mode MESFET process with double-level metal interconnect. The book documents the minimum geometries needed to yield functional devices, and it details the basic device structures that augment the construction of circuit elements. With the aid of the manual, a designer can then submit a database tape in a Calma GDSII format to the fabrication facility. The manufacturer offers two foundry services: a full foundry for production runs providing devices in wafer form, as loose die, or as packaged and tested devices; and a partial service, which permits the purchase of a portion of a wafer on a multiproject test chip to reduce nonrecurring charges. $500, including any updates released in the next two years.

Honeywell Inc, Gallium Arsenide IC Product Ctr, 830 E Arapahoe Rd, Richardson, TX 75081.

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Directory references VME Bus products

The winter 1986 edition of the *VMEbus Compatible Products Directory* contains an expanded cross-reference and lists over 1500 devices from more than 150 companies. This

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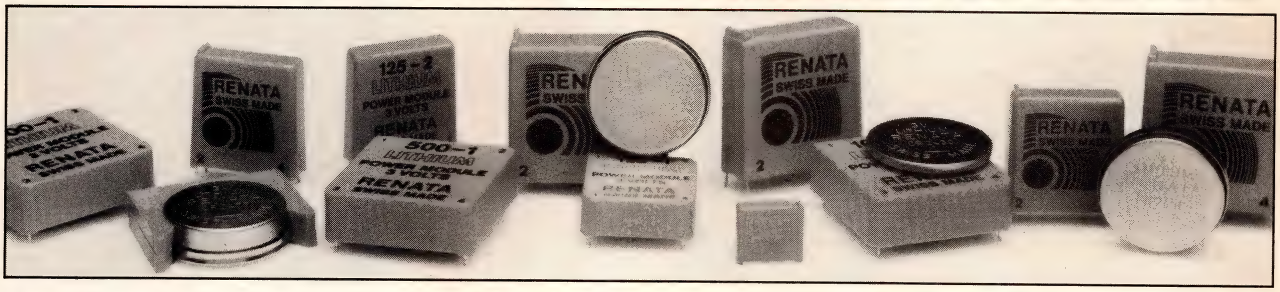

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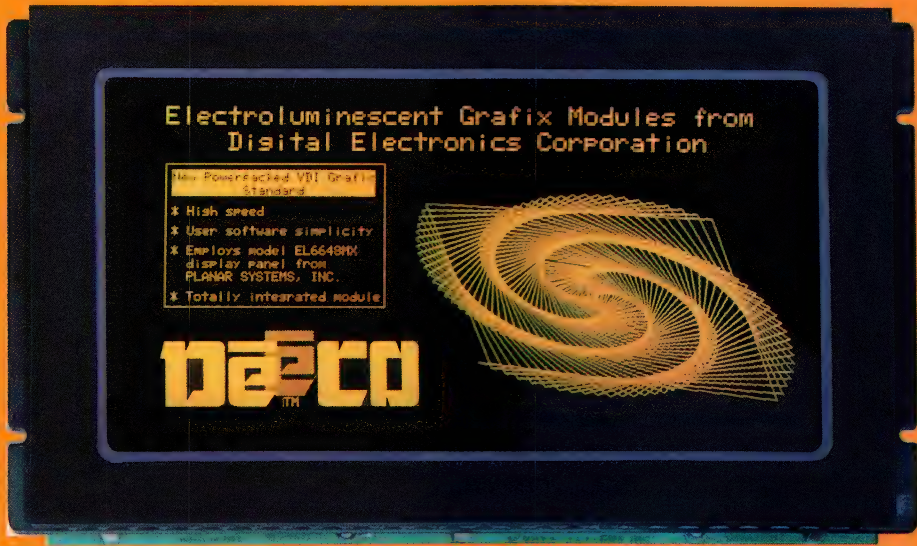

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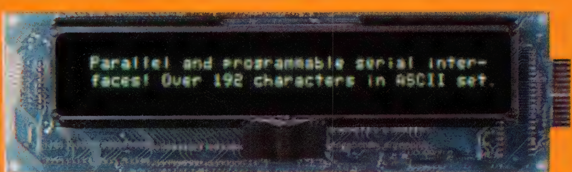
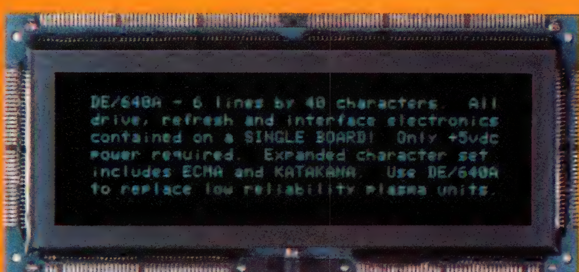


Vacuum Fluorescent Text Module allows 80 characters to be displayed. Only +5 vdc power needed. Same features as display below.

Vacuum Fluorescent Text Module, 40 characters. Same form factor as 2 lines x 40 characters display at left. RS-232 voltage levels optional on all VF display modules.



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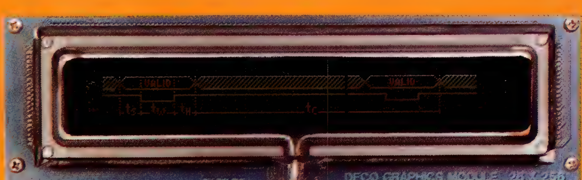

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compilation is 50% larger than the midyear 1985 edition and features μC boards, subsystems, bus interfaces, software, hardware packaging, and accessories. The directory costs $14.95 in the US and $19.95 outside the country.

VITA, 10229 N Scottsdale Rd, Suite E, Scottsdale, AZ 85253.

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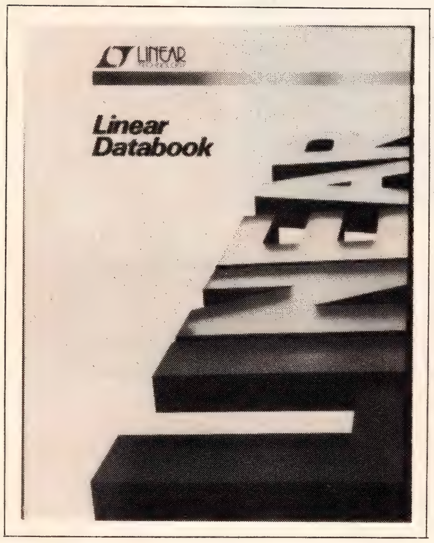


Booklets present MIL qualifications, products

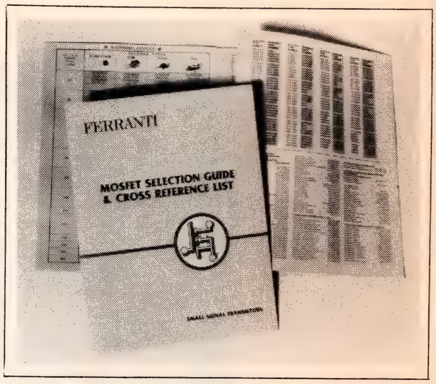
Two booklets present data on this company, its military linear products, and its qualifications as a supplier of military-specified devices. *Linear Databook*, a 768-pg catalog, covers commercial as well as MIL-qualified linear parts, including op amps, voltage regulators and references, comparators, filters, PWMs, data converters, and interface ICs. Each product-category section contains data sheets, electrical characteristics, and applications ideas for individual parts. The other brochure briefly traces the history of military-IC specifications and explains the manufacturer's spec system, quality policies, and procedures for complying with MIL-Q-9858, -I-45208, -M-38510, and -STD-883.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

Circle No 425

Guide to choosing MOSFETs

The *MOSFET Selection Guide and Cross Reference List* is a 6-pg document that includes information on traditional n-channel devices as well as design data on complementary n- and p-channel transistors. Organized in chart form, it provides parameter data on more than 170 MOSFET types housed in TO-92, TO-39, TO-220, and surface-mount SOT-23 packages. Typical parameters discussed include continuous current, on-resistance, and breakdown voltage. As its title implies,



the guide also contains a cross-reference of equivalent—or near-equivalent—devices to existing MOSFET types.

Ferranti Semiconductors, 87 Modular Ave, Commack, NY 11725.

Circle No 426

Handbook addresses fault-location methods

The subject of this applications handbook is fault location on 8-bit μP-based systems, including the Z80, 6800, 6502, 8085, 6802, 6809, and 1802. The book presents fault-location methods using the company's B2000A microprocessor bus tester and compares those methods with an emulator system's or logic probe's methods.

Miltex International, 502 W Wrightwood, Elmhurst, IL 60126.

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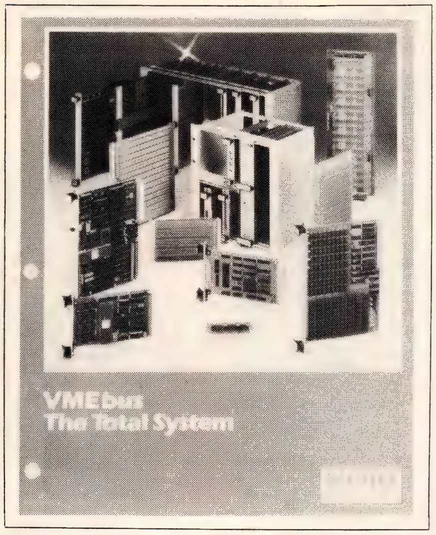

Catalog examines VME Bus components

Comprising 36 pages, this catalog details the company's VME Bus components, including 68000 CPUs, high-density static and dynamic memories, peripheral and communications interfaces, and analog input and output functions. In addition, a line of VME Bus backplanes and card frames, prototype boards, and power supplies support the components cataloged. Photos and diagrams supplement the text.

BICC-Vero Electronics Inc, 40 Lindemann Dr, Trumbull, CT 06611.

Circle No 428

Catalog examines test, measurement devices

This tabloid-format catalog presents a line of test and measurement peripherals for IBM, IBM-compatible, Apple, and Commodore personal computers, including digital oscilloscopes, spectrum analyzers, data loggers, and data-acquisition systems. The catalog contains specifications, sample CRT photos, and typical operator manual pages. In addition, it has a section pertaining to commonly asked questions regarding personal-computer-based test and measurement instruments and an applications chart.

Rapid Systems Inc, 755 N Northlake Way, Seattle, WA 98103.

Circle No 429

Catalog highlights semiconductor chips

This expanded 36-pg catalog describes the manufacturer's discrete semiconductors and wafers. Additions to the booklet include junction FETs, power transistors, power diodes, Schottky diodes, and several bipolar transistor geometries. Tables present data on electrical characteristics such as current gain, $V_{CE(sat)}$, and f_T. The catalog also contains dimensional drawings and packaging-option illustrations. It is 3-hole punched for loose-leaf filing.

Sprague Electric Co, Box 9102, Mansfield, MA 02048.

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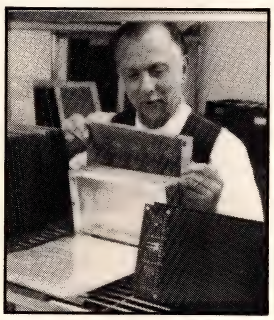

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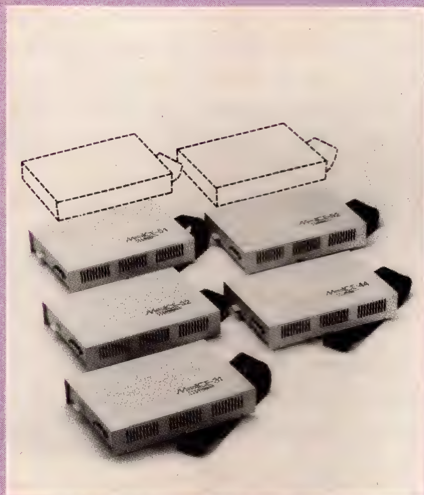

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Engineering students name companies for which they'd most like to work

Deborah Asbrand, *Staff Editor*

IBM, Hewlett-Packard, General Electric, and Hughes Aircraft are electrical-engineering students' top choices for the employer they'd like to work for after graduation. Three of the four companies have been long-time favorites with college students, having also been favored in similar surveys conducted in 1983 and 1981 by *Graduating Engineer* magazine in collaboration with the New York, NY, market-research firm Deutsch, Shea, and Evans.

Although IBM, Hewlett-Packard, and General Electric have been consistent winners with students, other corporate stars regularly rise and fall. Hughes Aircraft's ascendancy, for example, is the most dramatic of any company rated among the top 50 employers by students polled in 1985's survey. After landing in the twenty-first position in the 1981 poll, Hughes, buoyed by its reputation as a leader in the development of advanced electronics systems, rose to the number five spot in 1983, and became the fourth most sought-after employer in the 1985 study.

To secure fourth place on the list, Hughes overtook Texas Instruments, which lost some of its footing and dropped to number six. Other companies that tripped slightly in 1985 were Honeywell and Harris, falling from the seventh and eighth spots, respectively, to ninth and tenth.

Eying corporate financial health

Not surprisingly, students' level of interest in companies often parallels the companies' financial fortunes. When the demand for minicomputers declined last year, so did profits at Digital Equipment Corp, which posted losses for three consecutive quarters in 1985. Aware of the company's well-publicized troubles, students polled for the 1985 survey showed far less interest in going to work for the company than they had in previous surveys: Digital ranked ninth with students in the 1981 study and sixth in 1983, but stumbled to seventeenth in the 1985 poll.

Westboro, MA-based Data General, another minicomputer maker, suffered a fate similar to that of Digital Equipment Corp. Reports of plant shutdowns and massive layoffs weren't lost on students: The company occupied the number 20 spot in 1981 and the number 22 spot in 1983, but didn't make the top 50 list in 1985.

Motorola, riding the crest of the semiconductor boom, sprang from the number 16 position in 1981 to number seven in 1983. When the industry took a sharp downturn last year, so did students' interest in Motorola, which dropped to number 19 on the list. Other semiconductor manufacturers also fell out of favor with students. Intel slipped from the number 15 spot in 1983 to the

EE STUDENTS' EMPLOYER PREFERENCES*

	1985	1983
IBM	1	1
HEWLETT-PACKARD	2	2
GENERAL ELECTRIC	3	3
HUGHES AIRCRAFT	4	5
AT&T BELL LABS	5	6
TEXAS INSTRUMENTS	6	4
ROCKWELL	7	7
AT&T, ALL OTHER	8	18
HONEYWELL	9	7
EASTMAN KODAK	10	19
HARRIS	10	8
BOEING	11	19
LOCKHEED	12	15
NASA	13	17
TRW	14	11
GTE	15	10
WESTINGHOUSE	15	8
GENERAL MOTORS	16	16
RCA	16	12
DIGITAL EQUIPMENT	17	6
MARTIN MARIETTA	17	20
MOTOROLA	17	7
GENERAL DYNAMICS	18	14
MCDONNELL DOUGLAS	19	9
SPERRY	19	13
BELL COMMUNICATIONS RESEARCH	20	#
FORD	21	17
NORTHROP	21	21
US NAVY	22	15
SINGER	23	20

number 25 spot in 1985, and National Semiconductor dropped off the 1985 list of top 50 employers altogether.

Advanced Micro Devices' well-publicized no-layoff policy may be responsible for its changing fortunes with electrical-engineering students. The company, not listed in either the 1981 or 1983 studies, climbed up to number 26 among students polled for the 1985 list.

Influences on students' choices

In addition to tallying the companies students would most like to work for, the survey asked the students what factors influence their impressions of potential employers. Corporate planners will be happy to hear that students say their encounters with company representatives wield the greatest amount of influence over the company images they form. Some students also take into account advertisements, open houses, and career brochures, but generally to a much lesser degree.

Unhappily for many companies, influences that stretch beyond company control are growing in importance and diffusing the effects of the corporate-controlled image makers. Increasingly important to students are the articles they read in newspapers and magazines and the opinions of their friends and relatives.

In fact, a growing percentage of students polled say they now use media reports to form their impressions of corporations. Forty-eight percent of the students who responded say news reports and articles about companies contribute to the images they form about potential employers—an increase of 6% from the 1983 survey. Opinions of friends and relatives, which were important to 29% of students in 1983, were named as important by 34% of those questioned in 1985.

The ways in which electrical-engineering students of all disciplines form their opinions of potential employers is changing, but the reasons behind their choices remain consistent. The nature of the work they will be doing and a company's technical reputation are the two most important factors in students' choices of employers. Thirty-four percent of the students ranked the work they will be doing as their most important criterion; 22% of the students chose a corporation's technical reputation as the second greatest influence on their choice of employer.

Ranking a distant third on the list were advancement opportunities, which only 8% of the students polled mentioned. Students' mild concern with the advancement opportunities that will be available to them indicates an area where better career counseling is needed. Recent surveys of industry engineers have shown that poorly defined promotional paths are common and tend to be a source of great frustration.

Once students choose the company for which they would most like to work, they take active measures to secure a job there. In fact, the survey indicates that 13% had already accepted a position with their top choice when they filled out the questionnaire. Two percent had taken jobs with their second-place choice, and another 2% had accepted job offers from their third-choice company. Of those students who hadn't yet accepted a position, 65% had submitted resumes to their favored employers, and more than half had scheduled interviews or were expecting to do so soon. **EDN**

Section Interest Quotient
(Circle One)
High 518 Medium 519 Low 520

	1985	1983
US AIR FORCE	23	#
XEROX	23	22
BURROUGHS	24	22
NCR	24	21
INTEL	25	15
NEC ELECTRONICS	25	#
3M	25	22
ADVANCED MICRO DEVICES	26	#
DU PONT	26	23
E-SYSTEMS	26	18
GRUMMAN	26	22
ITT	26	18
UNITED TECHNOLOGIES	26	18
ELECTRONIC DATA SYSTEMS	27	#
NATIONAL SECURITY AGENCY	27	#
RAYTHEON	27	20
SCHLUMBERGER	27	19
TEKTRONIX	27	#
BECHTEL	28	21
EXXON	28	#
M/A-COM	28	#
MONSANTO	28	#
NORTH AMERICAN PHILIPS	28	#
OWENS-CORNING FIBERGLASS	28	#
PROCTER & GAMBLE	28	#
WANG	28	20

*TIES RESULT IN TOTAL OF MORE THAN 50 CORPORATIONS.
#NOT CHOSEN AS ONE OF TOP 50 EMPLOYERS.
(SOURCE: DEUTSCH, SHEA, AND EVANS, NEW YORK, NY)

Sergio Roffo

CAREER OPPORTUNITIES

1986 Editorial Calendar and Planning Guide

EDN

EDN CareerNews

Issue Date	Recruitment Deadline	EDN Editorial Emphasis	EDN CareerNews
July 10	June 19	Product Showcase—Volume I; IDs & Semiconductors; Hardware & Interconnection Devices; Power Supplies/Sources; Software; Literature on Computers & Peripherals, Components, Test & Measurement Instruments, International Products	
July 24	July 2	Product Showcase—Volume II; Computers & Peripherals; Components; Test & Measurement Instruments; International Products; Literature on ICs & Semiconductors, Hardware & Interconnection Devices, Power Supplies/Sources, Software	
Aug. 7	July 17	Resistors; CAE; Communications ICs; Microprocessor Development Software; Technical Article Database Index	Closing: 8/14 Mailing: 8/26
Aug. 21	July 31	Military Electronics Special Issue; High-speed ICs; Communications Technology	
Sept. 4	Aug. 14	Test & Measurement Special Issue; Oscilloscopes; Automated Design & Engineering for Electronics Product Preview (CAE-related*); Meters; Display Technology	Closing: 9/11 Mailing: 9/23
Sept. 18	Aug. 27	Personal Computer-Based CAE; Power ICs; Computer Peripherals; Hardware & Interconnection Technology; EDN 30th Anniversary Tribute	
Oct. 2	Sept. 11	Surface Mount Technology; Memory ICs; CAE; Semicustom IC Directory (CAE-related*)	Closing: 10/16 Mailing: 10/28
Oct. 16	Sept. 25	Digital Signal Processing; Personal Computers; ICs; Test & Measurement Instruments; Display Technology	

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LOOKING AHEAD

EDITED BY GEORGE STUBBS

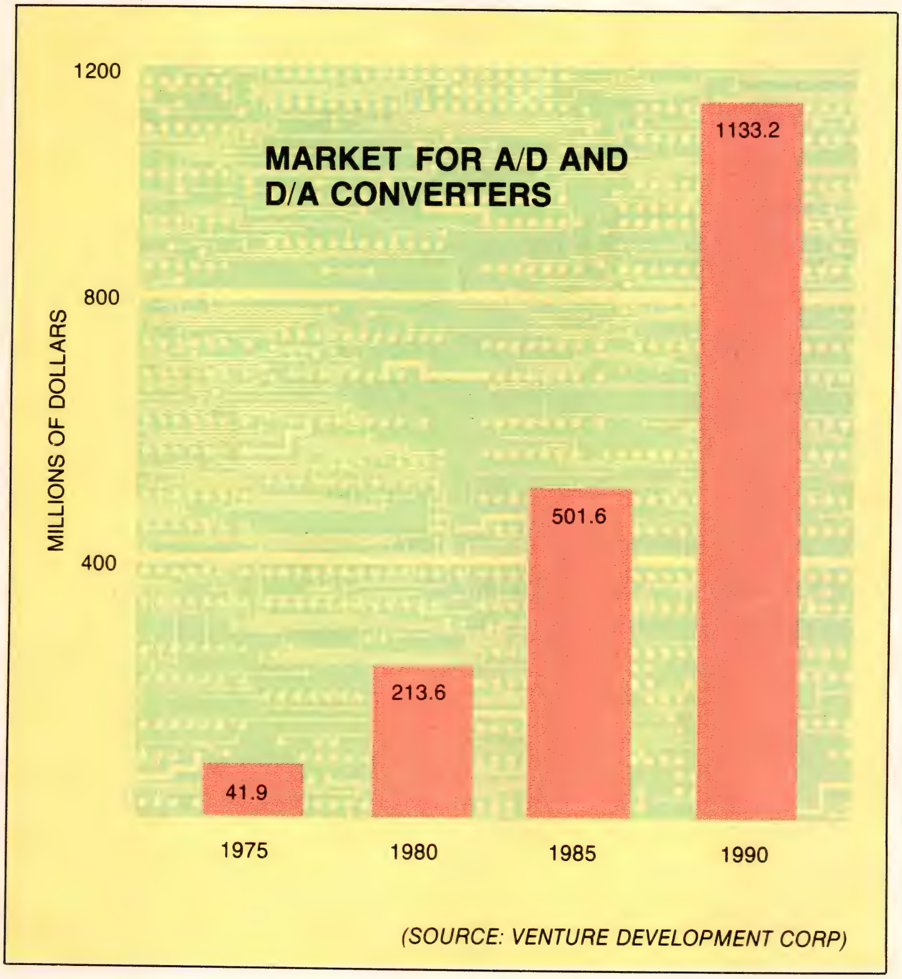
μPs to spur $1.13B market for data converters

The market for A/D and D/A converters continues to benefit from attempts to bring computer power to all kinds of data-acquisition applications. According to the market-research company Venture Development Corp (Natick, MA), the value of US shipments of these data converters will increase at an annual rate of 17.7%, from $501.6 million in 1985 to $1.13 billion by 1990.

A/D converters receive analog information from such devices as pressure, temperature, and distance transducers and convert this information into digital signals that a computer can store or analyze. D/A converters convert digital information into analog signals that control such devices as actuators, heating elements, pressure valves, and analog displays. Clearly, data converters and computers have a central role in any system that must respond to environmental changes.

The growth of the data-converter market has closely tracked the proliferation of the microprocessor. In 1975, data converters generated a mere $41.9 million in sales revenue, but they rode the crest of the μP wave and constituted a $214 million market in 1980. During that period and since, smaller, less-power-hungry monolithic D/A and A/D converters have gained in popularity compared with hybrid and modular types.

Monolithic technologies will continue to make advances, capitalizing on developments in CMOS and high-speed-bipolar processes. VDC reports that the use of hybrid converters in high-performance contexts will grow at a fast pace. Modular converters will not disappear; although they will continue to lose market share, they will exhibit some growth in specialized high-performance applications.



VLSI IC design centers to gain share of ASIC design

By 1990, regional VLSI IC design centers will be assisting 60% of all systems designers in the development of application-specific ICs (ASICs), according to Electronic Trend Publications (ETP), the Cupertino, CA-based market and applications research company. This level of assistance means that regional design centers will have a hand in 75% of all sales of ASICs in 1990.

Designers of electronic systems call upon the services of VLSI IC design centers as the result of a combination of factors. Large-system OEMs with the internal facilities to design ICs have aggressively employed full-custom VLSI design techniques, and recent advances in CAD/CAE technology have put such capability into the hands of smaller OEMs. Yet most OEMs, regardless of size, are beginning to notice that the pool of IC design talent is getting comparatively smaller.

ETP estimates that there are between 3000 and 4000 expert IC designers in the world, with nearly 65% of them employed by semiconductor manufacturers. This population has not changed appreciably for 10 years and will remain unchanged into the next decade, says ETP. By contrast, the number of system designers has tripled over the previous decade and is expected to double again by 1990. The familiar laws of supply and demand have put a premium on expert IC designers, and the emergence of VLSI IC design centers is directly linked to the shortage of such expertise.

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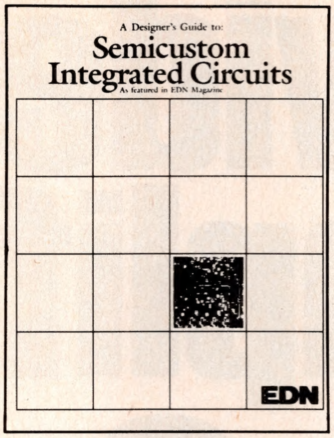

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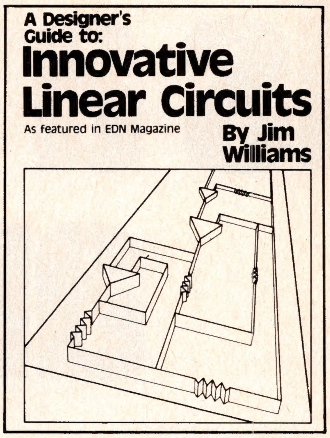

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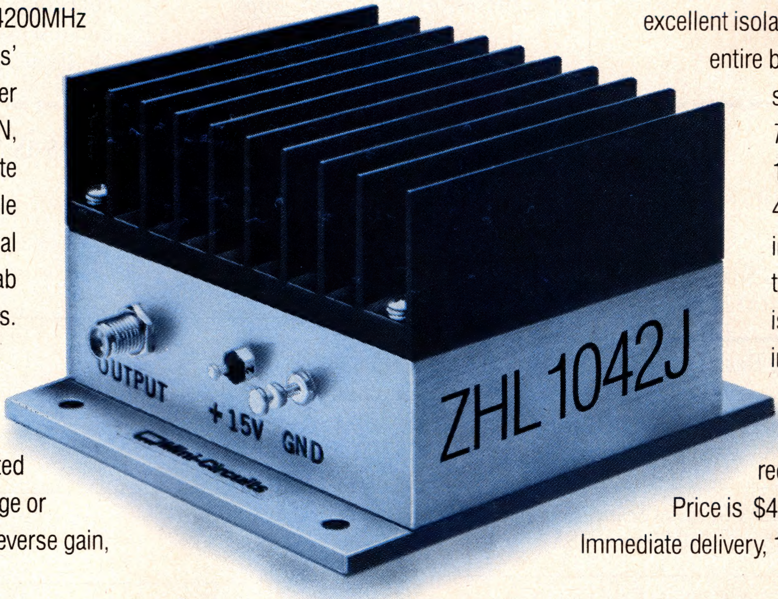

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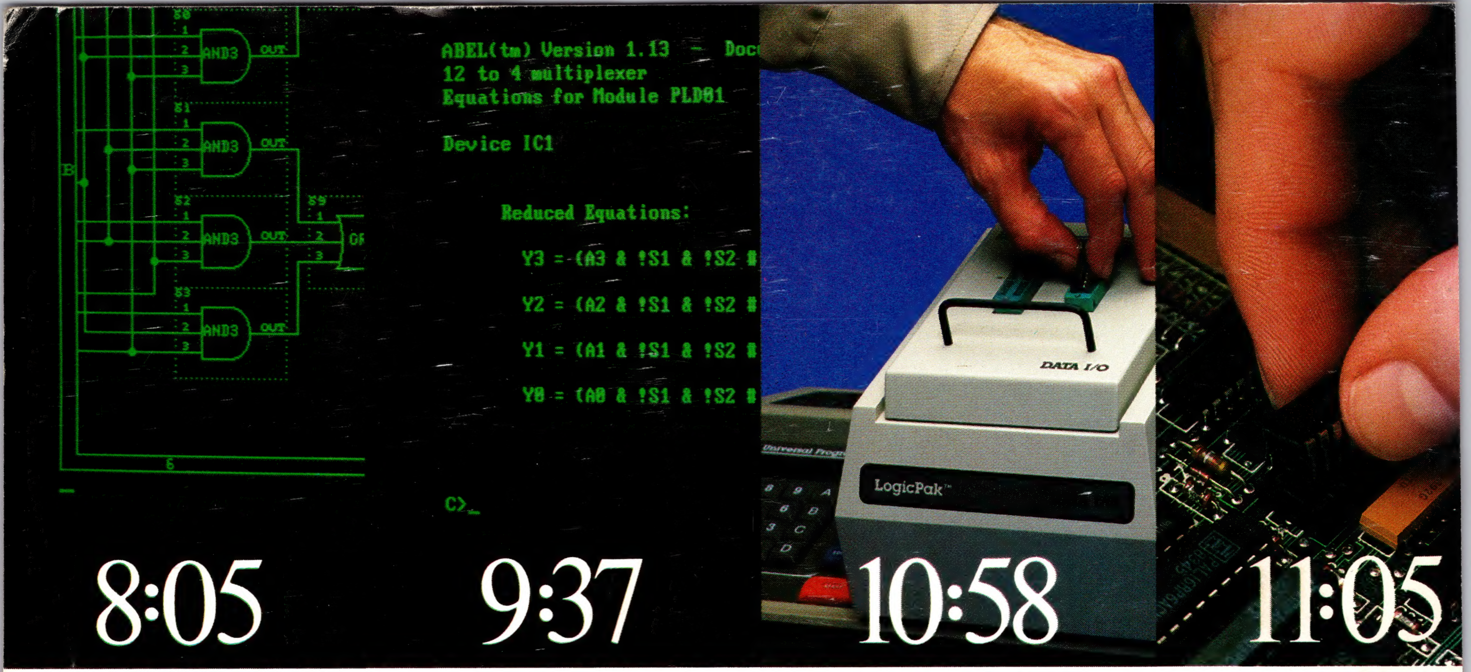


CONCEPT TO SILICON IN 3 HOURS FLAT.

ALL THE BENEFITS OF CUSTOM DESIGN WITHOUT THE WAIT. Sometimes, the only way to optimize a design is by using custom parts. But some application-specific integrated circuits (ASICs), like gate arrays, can take weeks to develop.

Programmable Logic Devices (PLDs) may be the right solution for your application. They offer low risk and high design flexibility to reduce your development costs.

LOGIC CONCEPT TO FINAL DEVICE RIGHT AT YOUR DESK. Data I/O's Personal Silicon Foundry gives you all the tools you need to take logic from concept to programmed device in just hours. The Personal Silicon Foundry, based on an IBM® Personal Computer, automates time-consuming tasks such as design, logic reduction, test vector generation and verification. You can easily experiment to optimize your design and quickly test each iteration in an actual circuit.

FOUR WAYS TO EXPRESS YOUR DESIGN. With our FutureNet DASH™ schematic design package and ABEL™, the industry-standard logic language, you can express your concept in any combination of schematics, truth tables, state diagrams or Boolean equations—whichever you prefer.

The Personal Silicon Foundry™

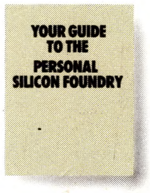
CREATE A FULLY TESTABLE DEVICE IN MINUTES. Because simulation is an integral part of the Personal Silicon Foundry, you can segment your logic circuit, develop test vectors and debug the design in one process. You can also automatically analyze design testability and generate device test vectors. The result: You easily produce a fully testable PLD.

SUPPORTS PLDS OF YOUR CHOICE. You have the flexibility to choose any PLD from virtually any manufacturer.

Select one of two Data I/O logic programmers to match your device requirements. Both give you full-functional testing and easy operation from the PC keyboard.

AUTOMATICALLY DOCUMENTS THE ENTIRE PROCESS. Throughout design, simulation, programming and testing, the Personal Silicon Foundry generates all necessary documentation. Your PLD is ready for the production line just hours after your concept is developed.

CONFIGURE YOUR OWN PERSONAL SILICON FOUNDRY. ASK US HOW. As the world leaders in PC-based CAE and PLD support tools, Data I/O and FutureNet* can help you tailor your own Personal Silicon Foundry. Call us today, toll free **1-800-426-1045** and ask for your free guide to PLDs and the Personal Silicon Foundry.



Capturing the power of PLDs is that simple. And fast.

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